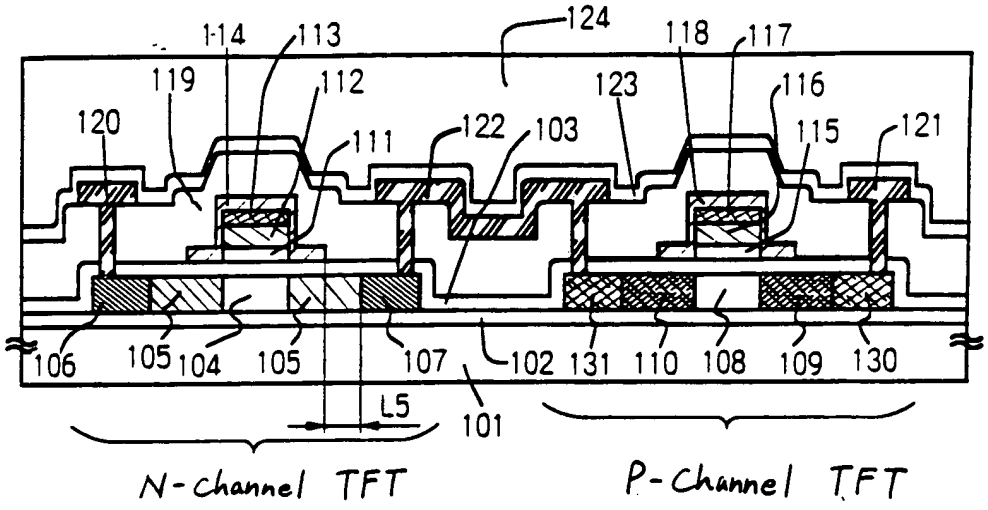

114
113
124
118
117
119
112
123
116
120
111
122
103
115
121
106
105
104
105
107
102
131
110
108
109
130
L5
101
N-channel TFT
P-channel TFT

Fig. 1

Fig. 2A

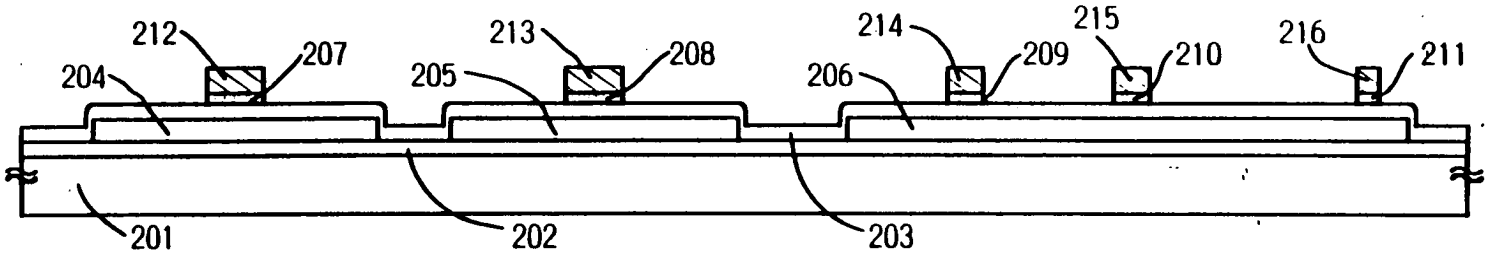


Fig. 2B

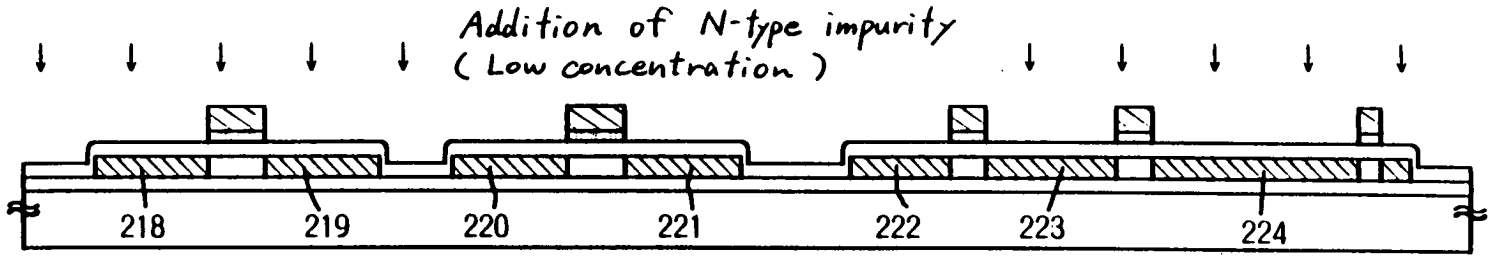


Fig. 2C

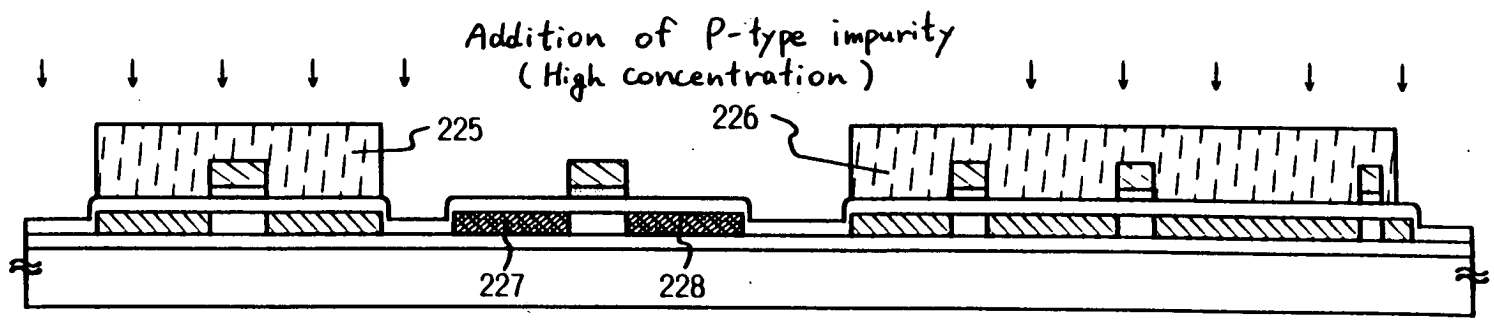


Fig. 3A

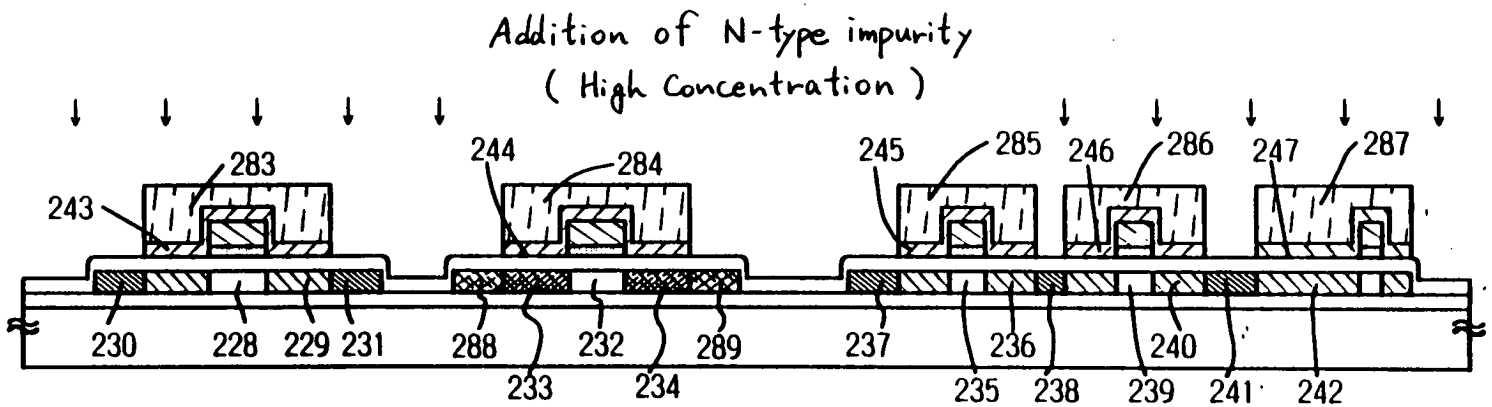


Fig. 3B

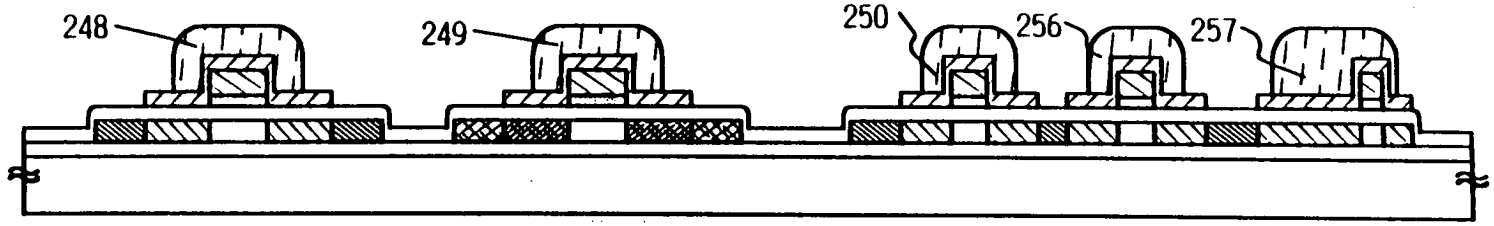


Fig. 3C

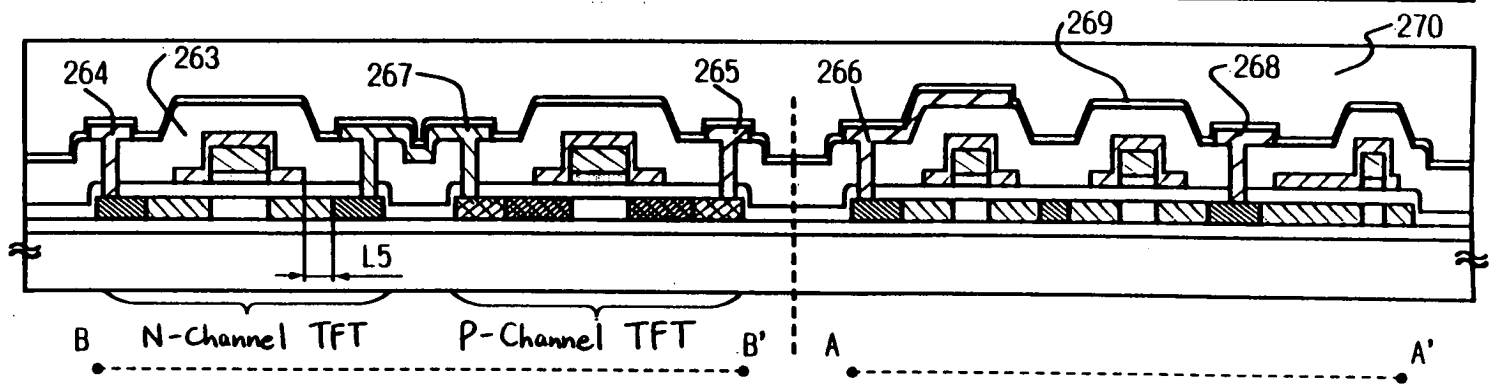


Fig. 4A

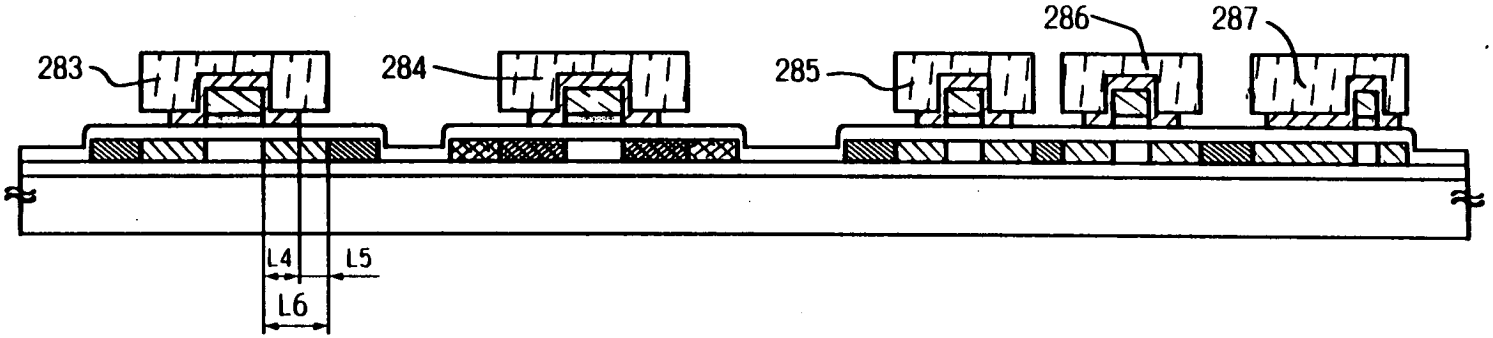

283
284
285
286
287
L4
L5
L6

Fig. 4B

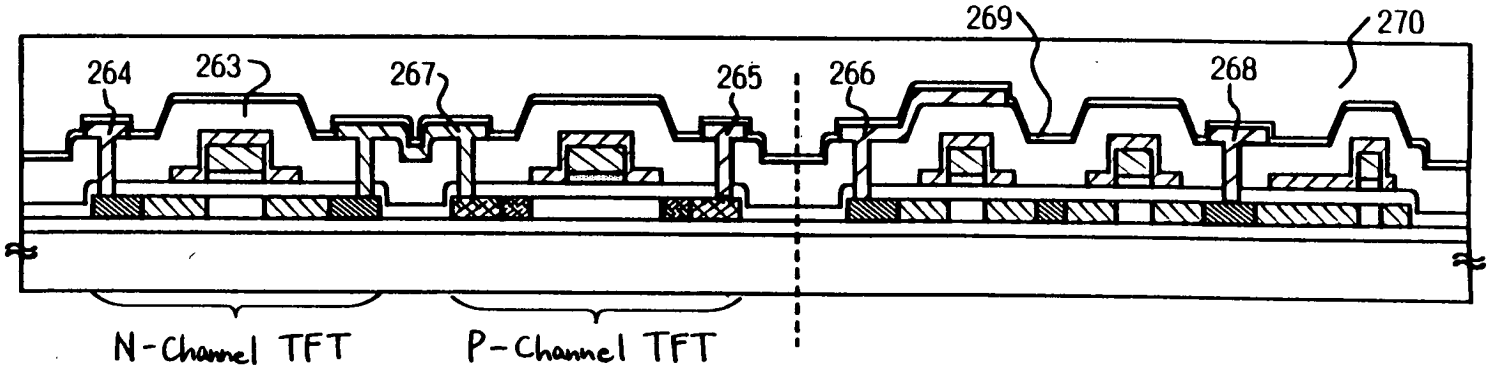

264
263
267
265
266
269
268
270
N-Channel TFT
P-Channel TFT
CMOS Circuit
Pixel Matrix Circuit

Fig. 5A

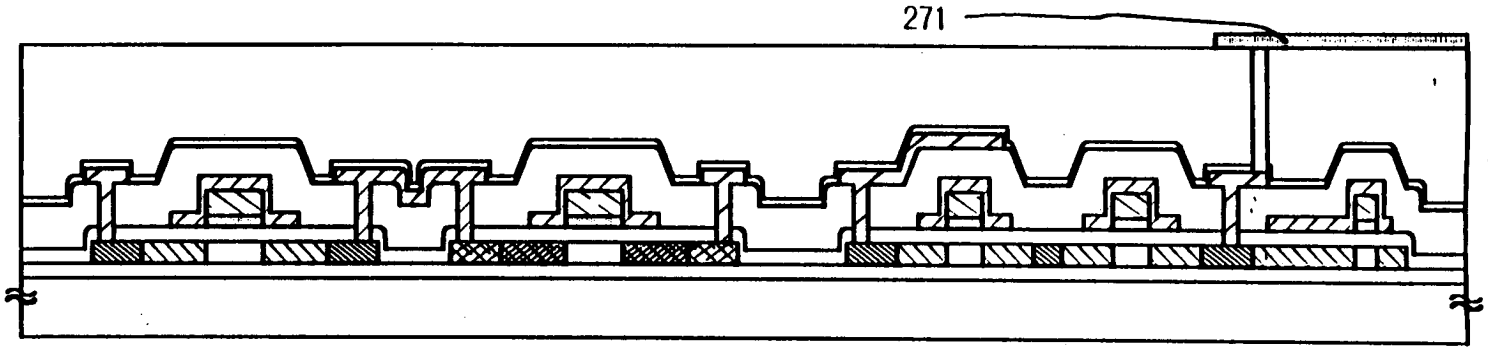


Fig. 5B

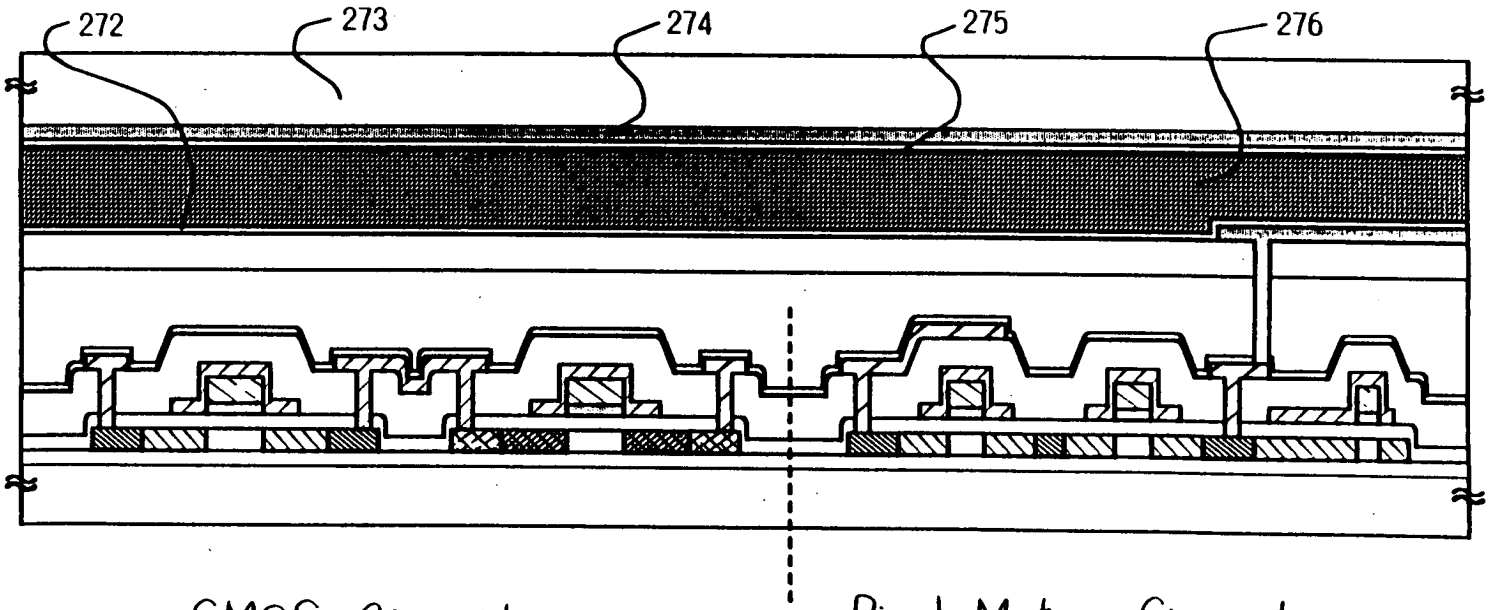


Fig. 6A

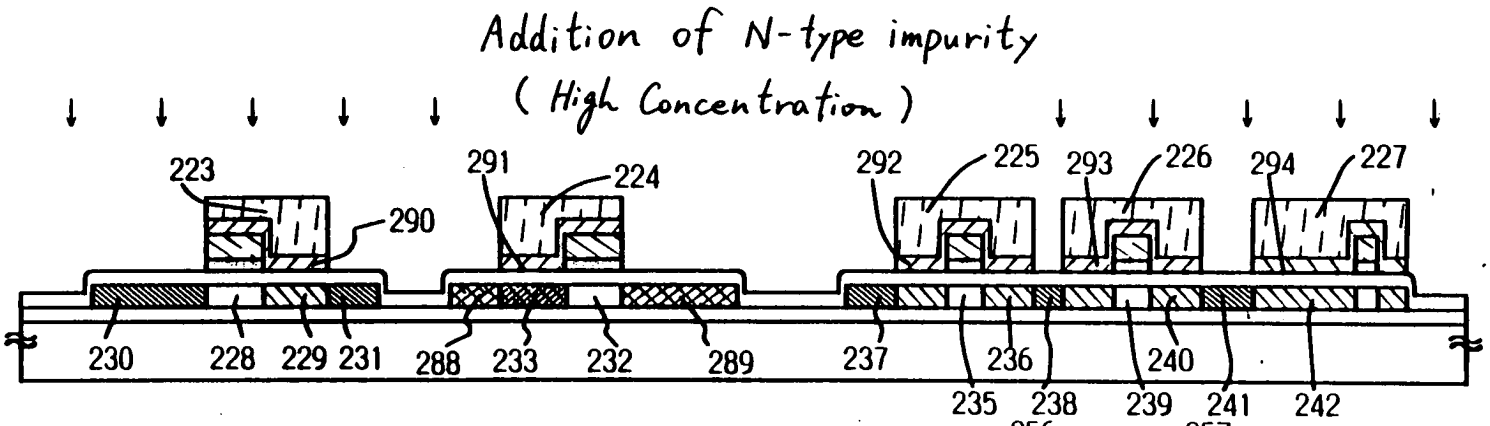


Fig. 6B

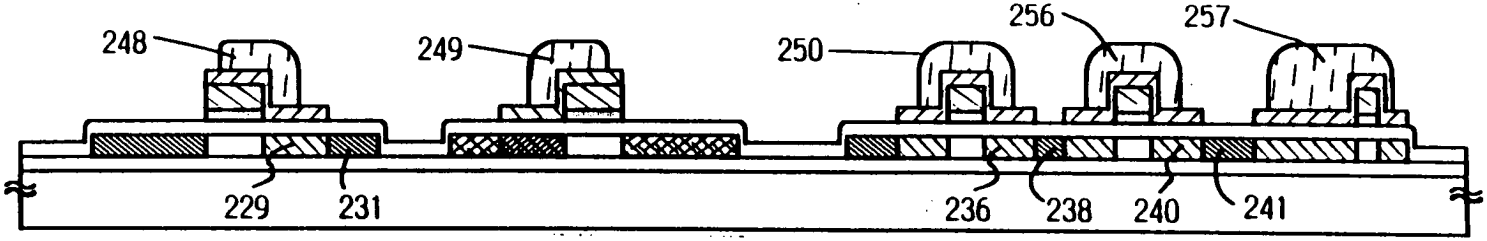
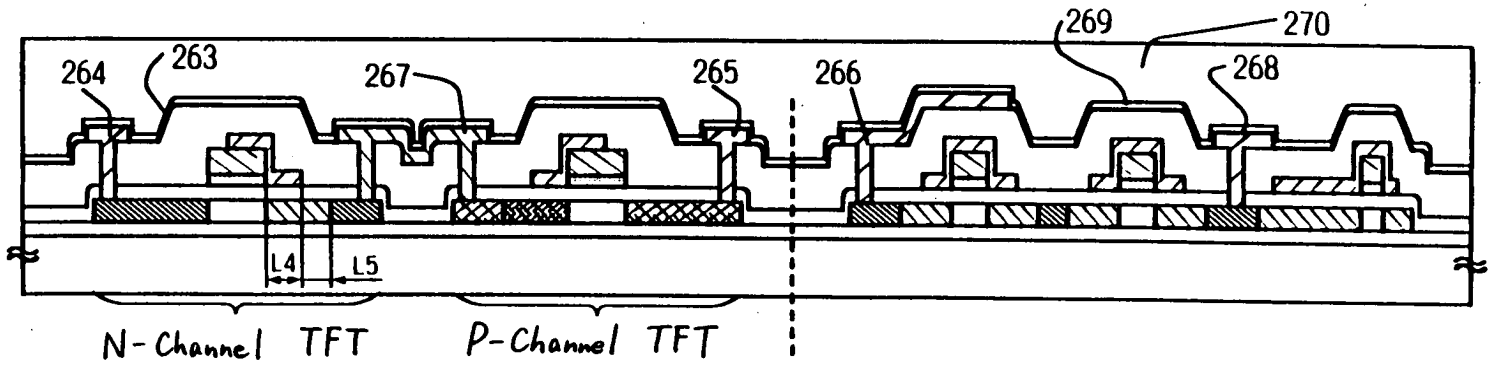


Fig. 6C



CMOS Circuit

Pixel Matrix Circuit

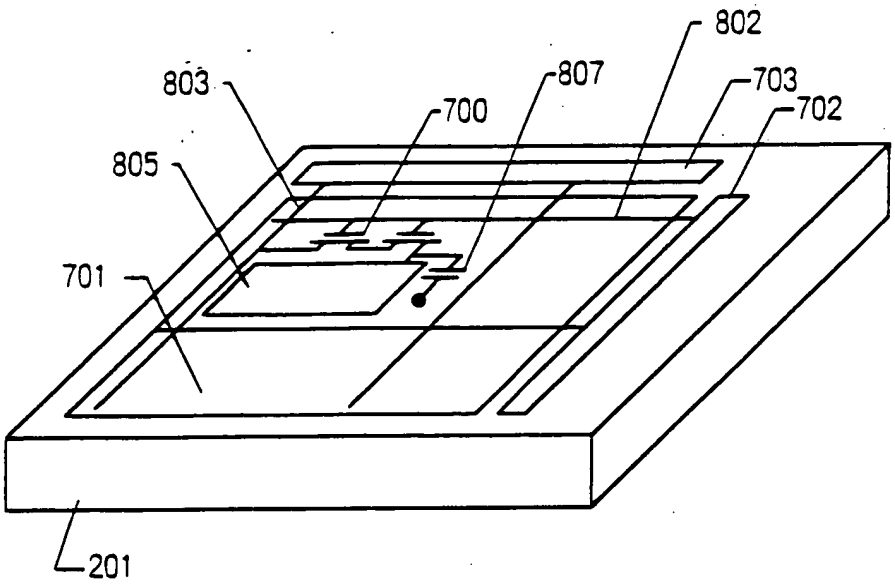


Fig. 7

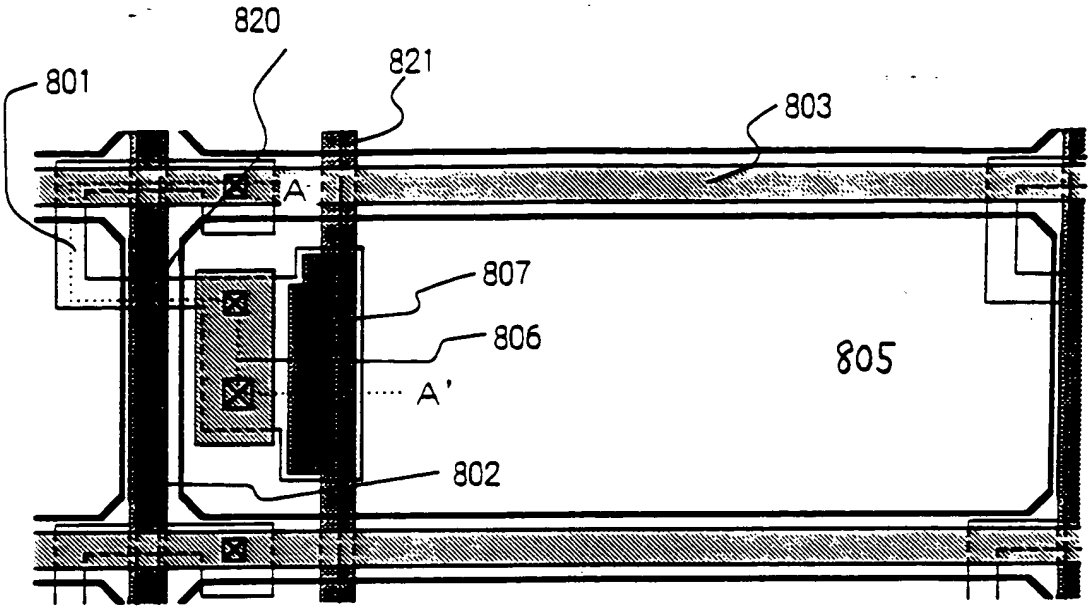

820
821
801
803
A
807
806
805
A'
802

Fig. 8A

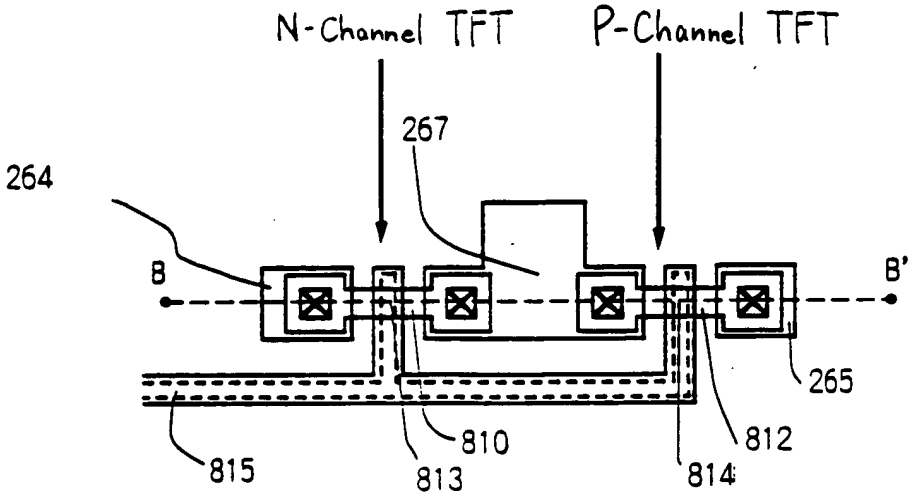

N-Channel TFT
P-Channel TFT
267
264
B
B'
265
810
812
815
813
814

Fig. 8B

Fig. 9A

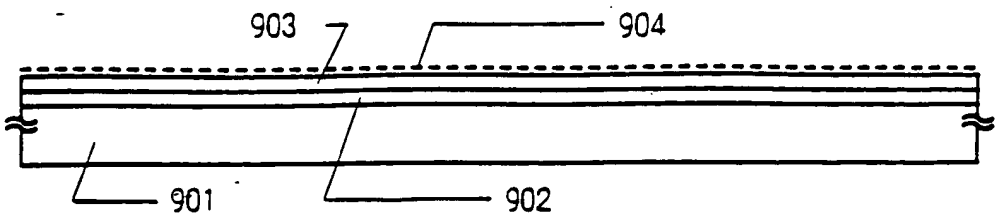


Fig. 9B

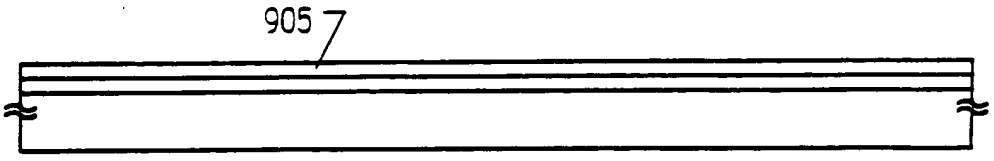


Fig. 10A

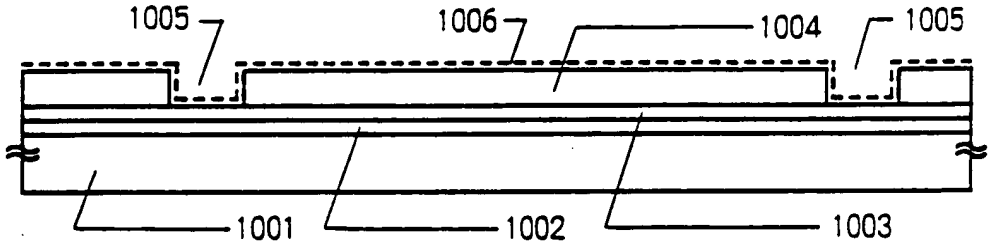


Fig. 10B

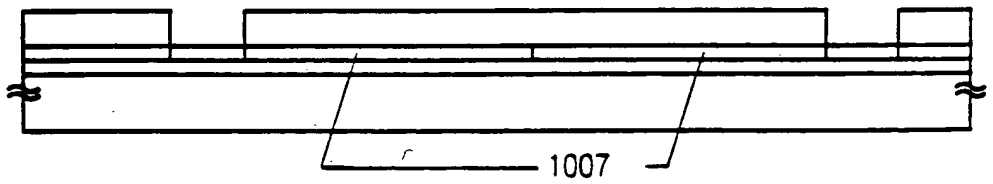


Fig. 11A

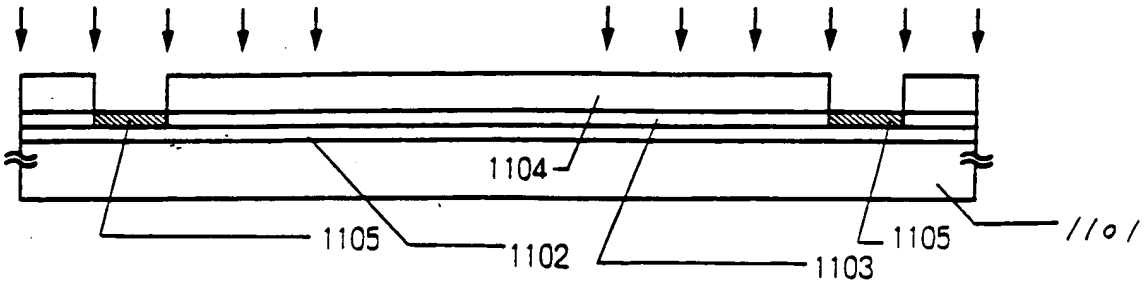


Fig. 11B

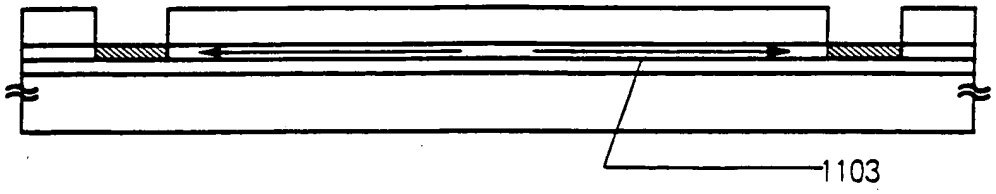


Fig. 12A

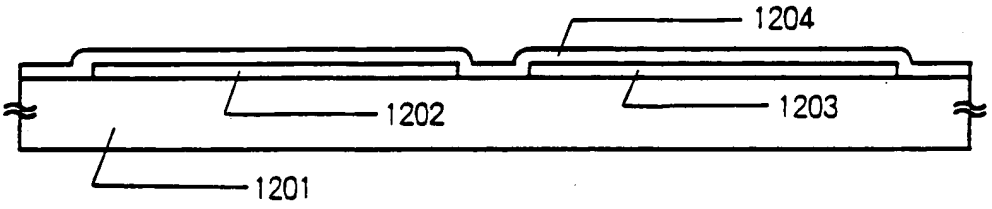
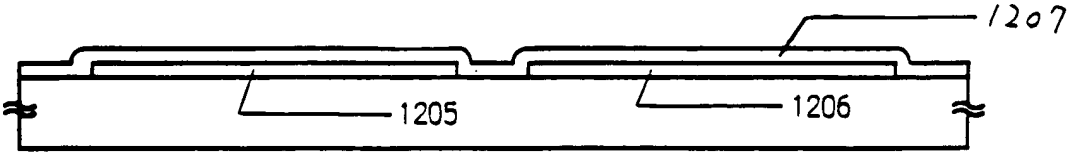


Fig. 12B



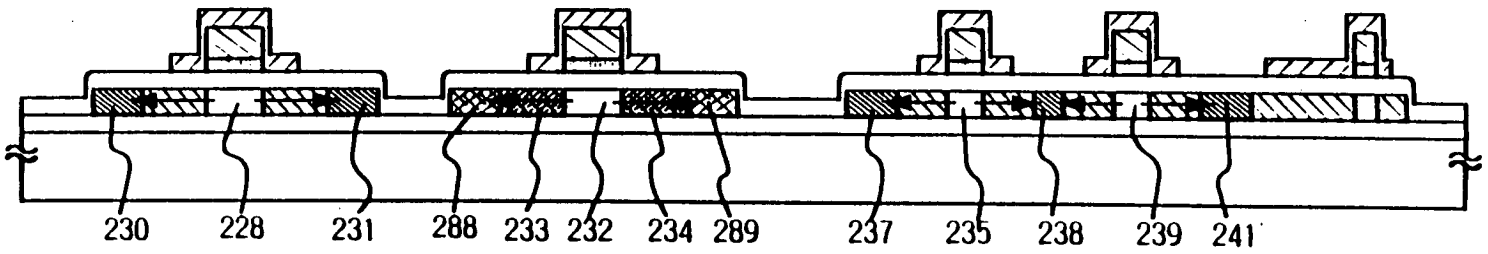


Fig. 13

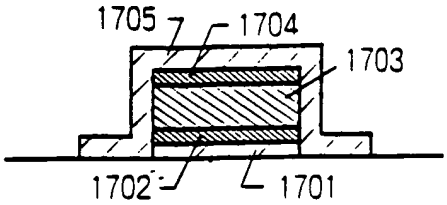


Fig. 14A

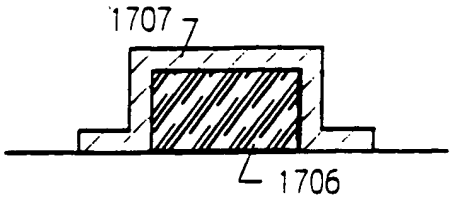


Fig. 14B

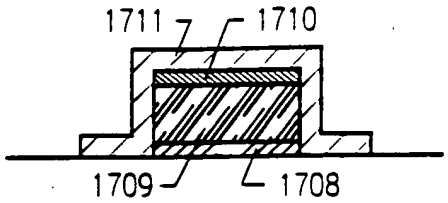


Fig. 14C

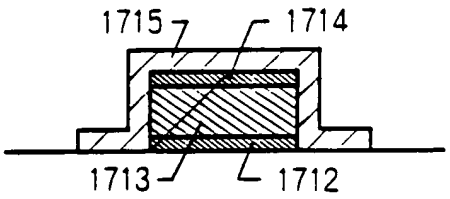


Fig. 14D

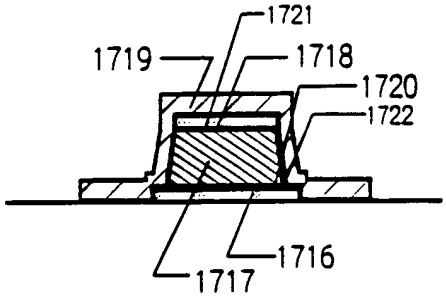


Fig. 14E

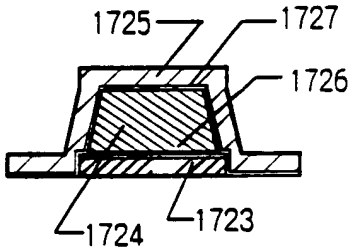


Fig. 14F

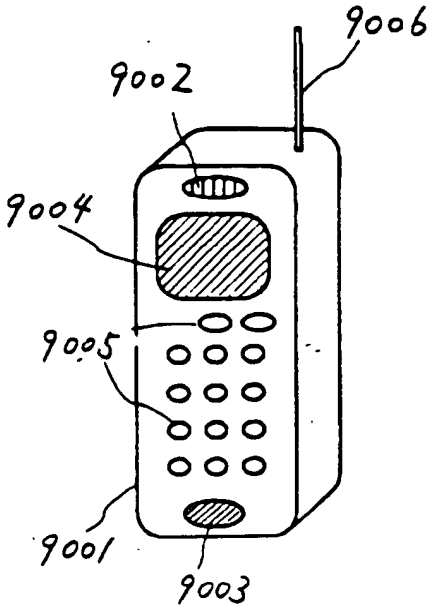


FIG. 15A

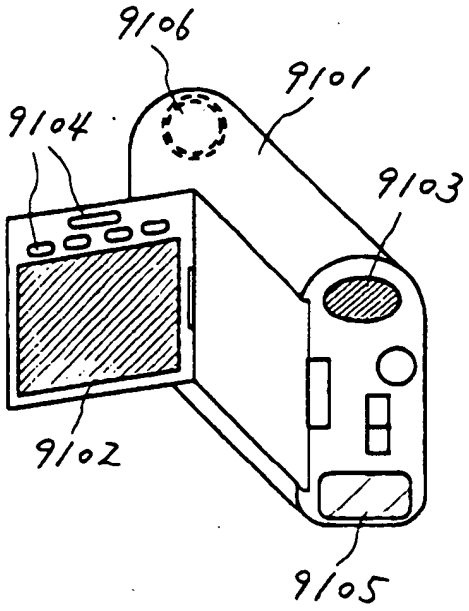


FIG. 15B

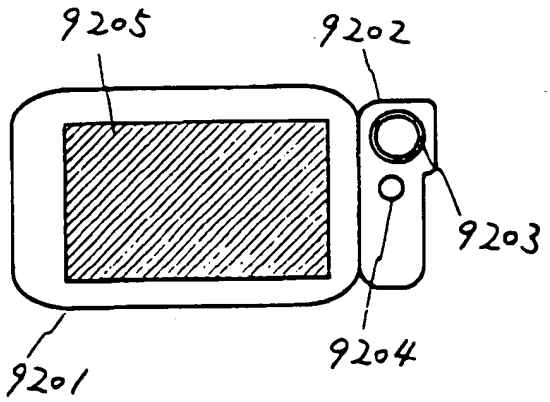


FIG. 15C

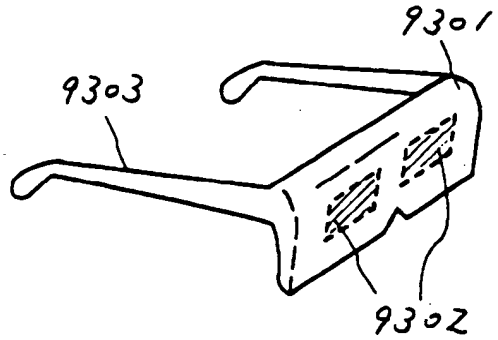


FIG. 15D

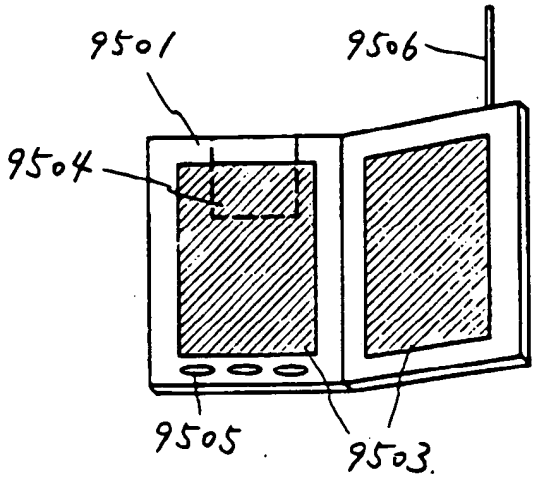


FIG. 15E

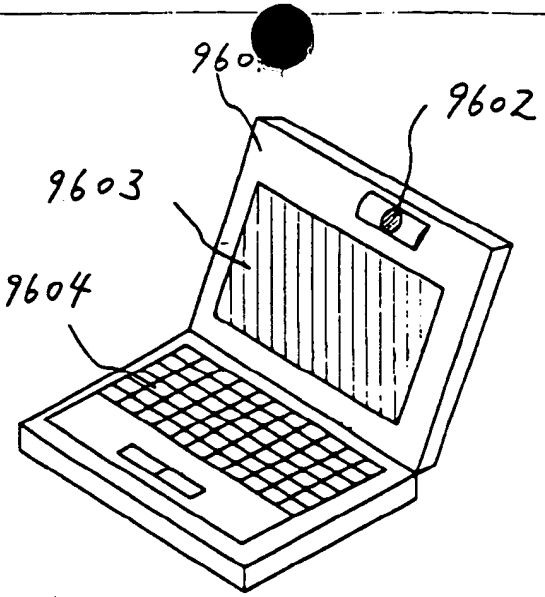


FIG. 15F

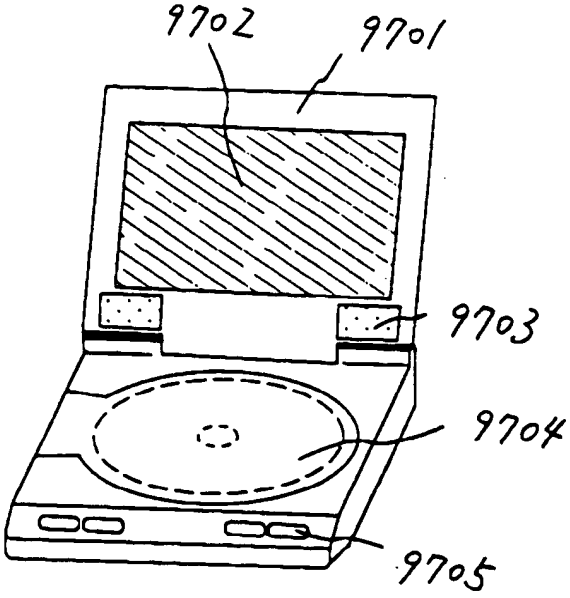


FIG. 15G

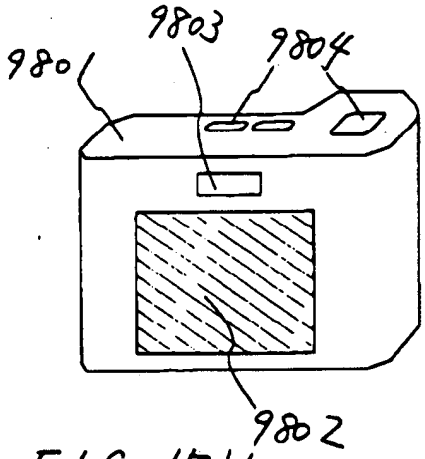


FIG. 15H

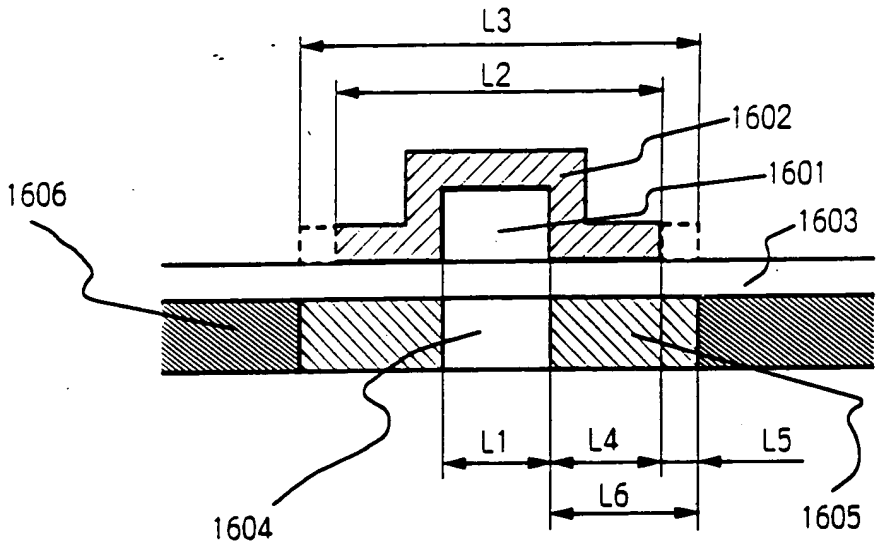


Fig. 16

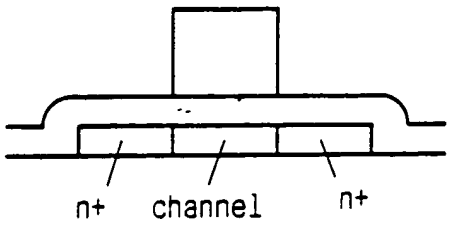


Fig. 17A-1

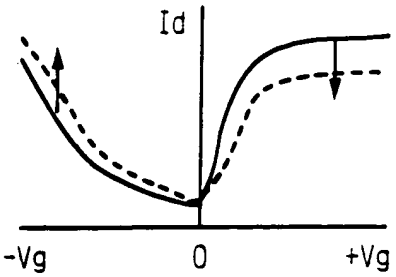


Fig. 17B-1

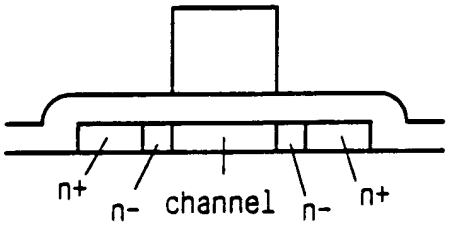


Fig. 17A-2

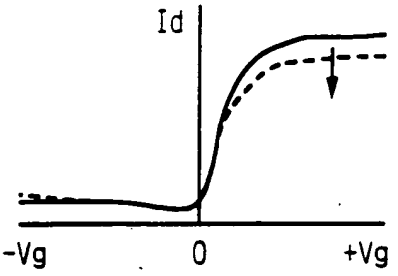


Fig. 17B-2

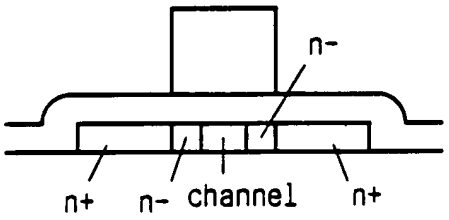


Fig. 17A-3

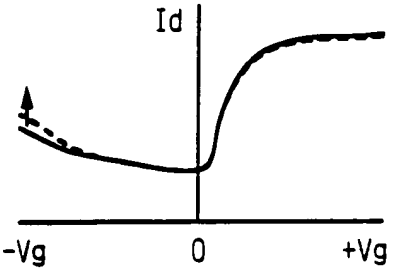


Fig. 17B-3

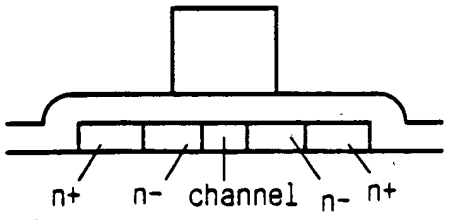


Fig. 17A-4

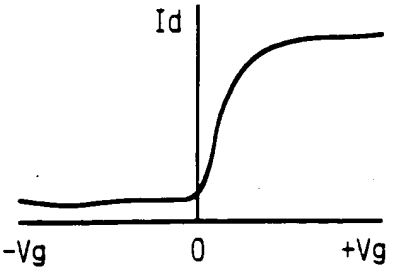


Fig. 17B-4

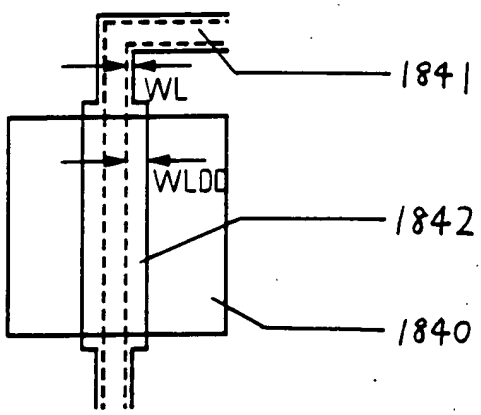


Fig. 18

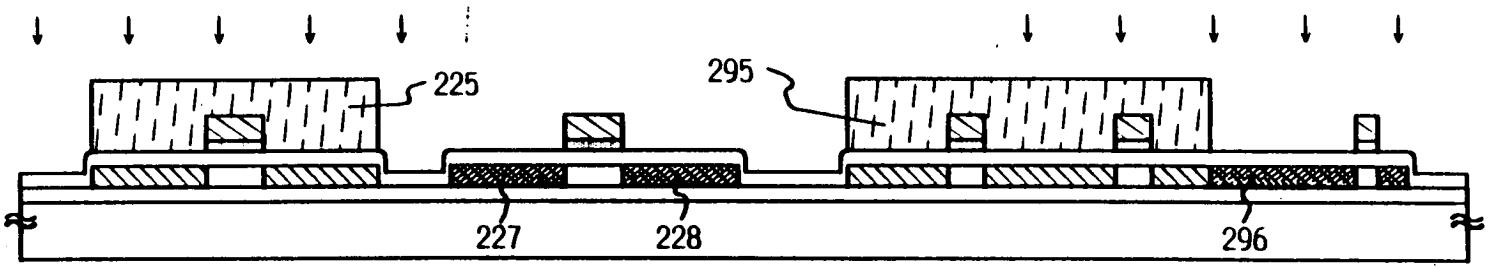


Fig. 19

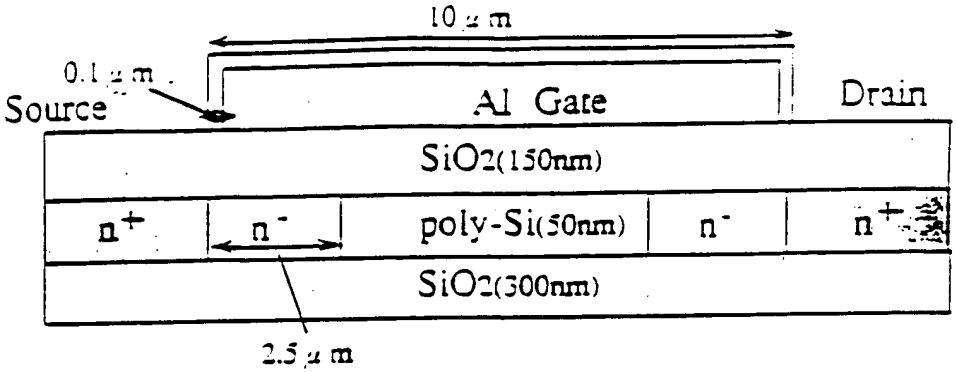
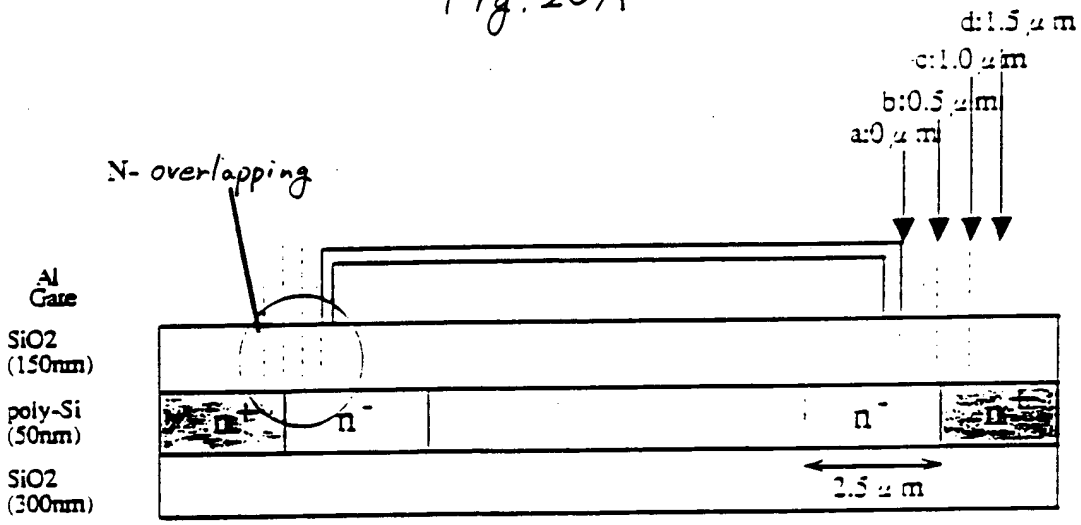


Fig. 20A

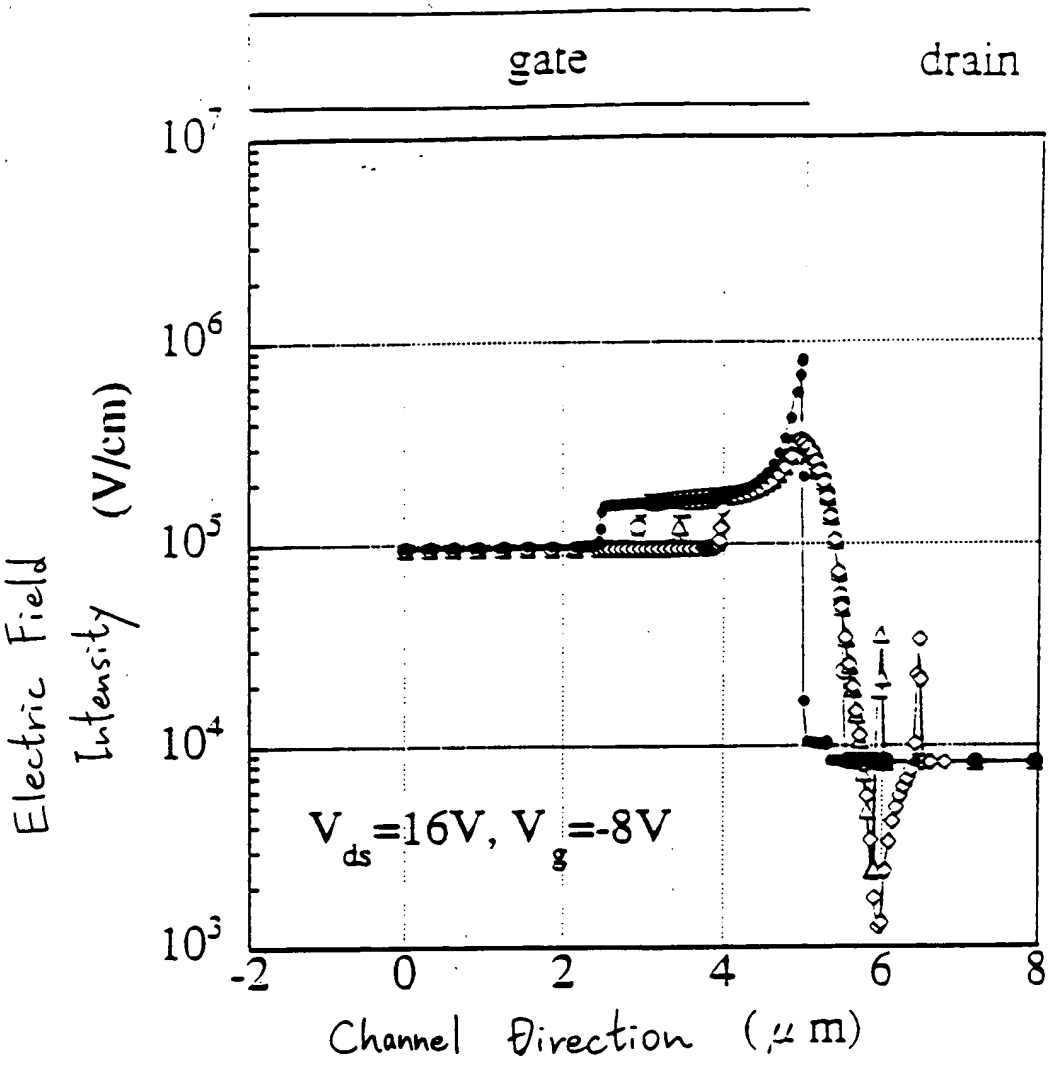


※ Width of n^- region is fixed in 2.5 μm.

Concentration of n^- region (activated conc.) : 4.2E17/cm3

Concentration of n^+ region (activated conc.) : 2E20/cm3

Fig. 20B



n⁻ concentration:4.2E17/cm³

—○— b: LDD 0.5 μm + GOLD 2.0 μm
—△— c: LDD 1.0 μm+ GOLD 1.5 μm
—◇— d: LDD 1.5 μm+ GOLD 1.0 μm
—●— a: LDD 0 μm + GOLD 2.5 μm

Fig. 21

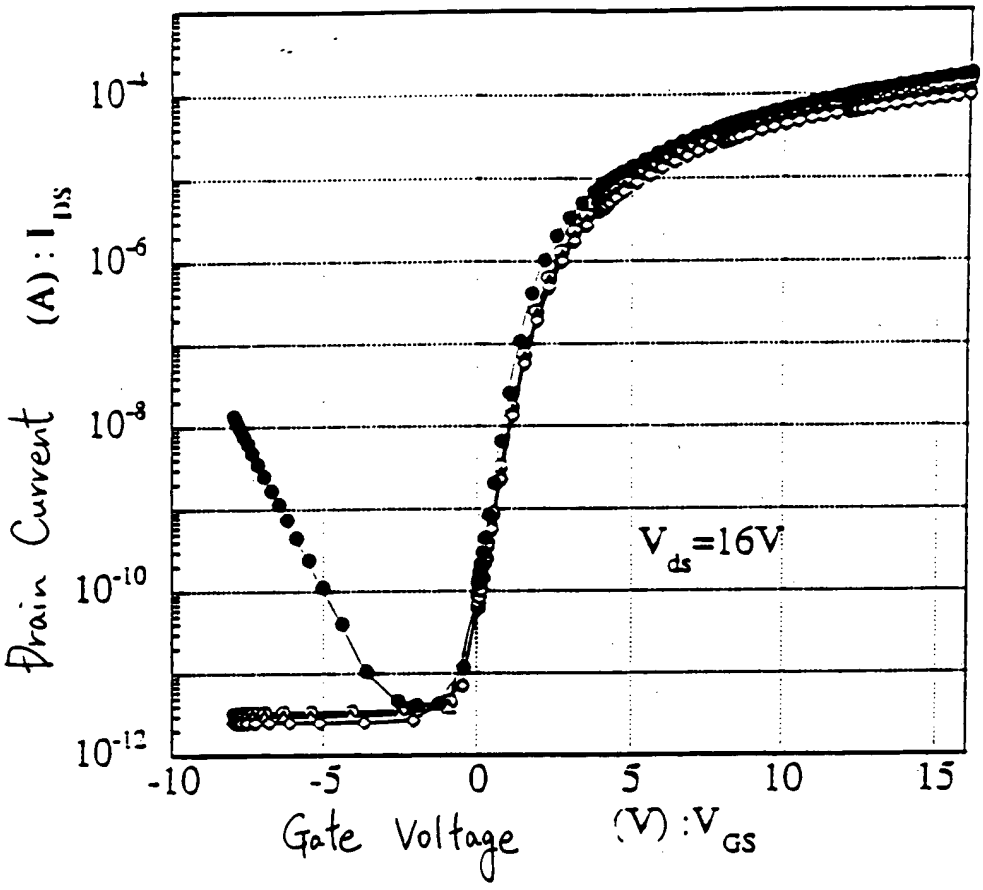
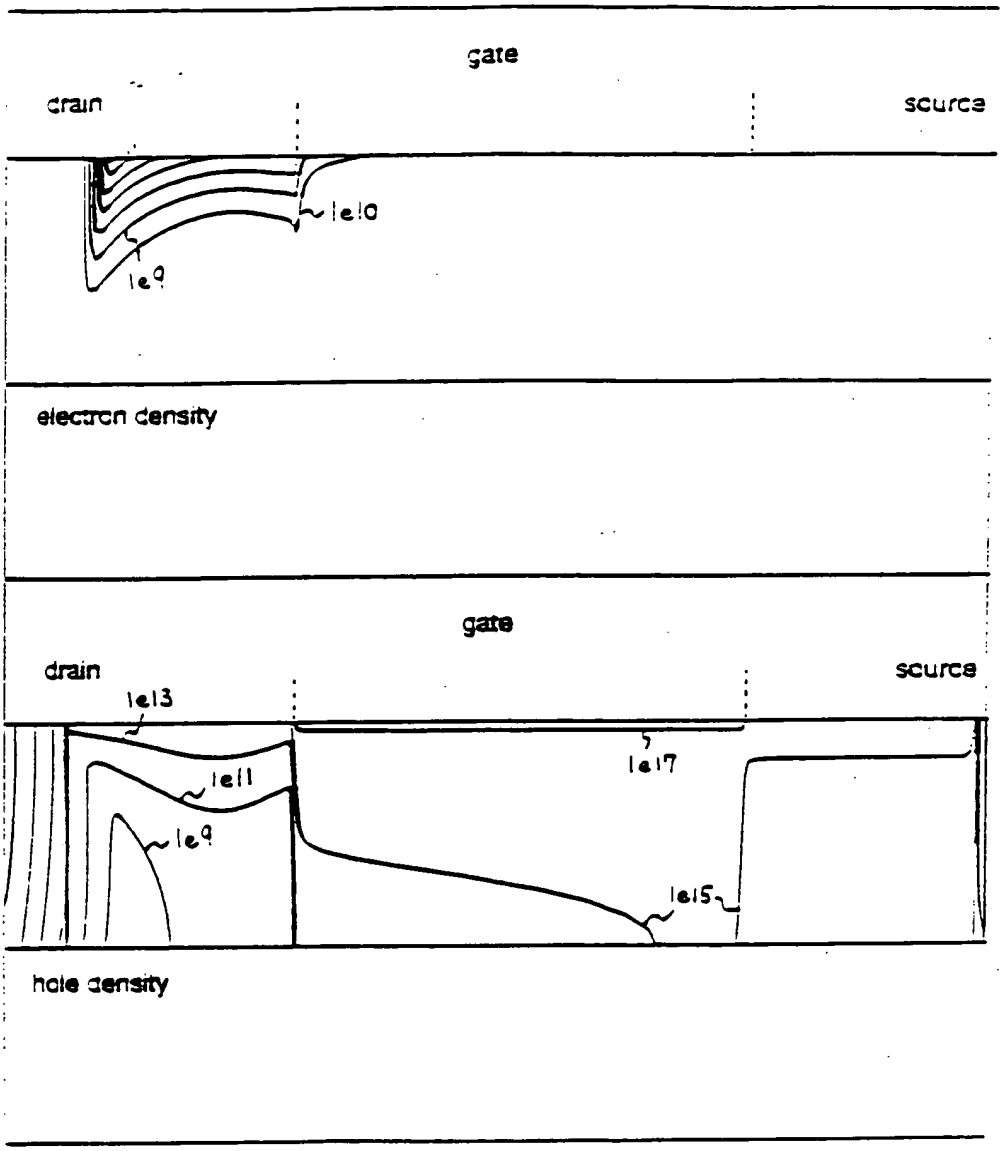
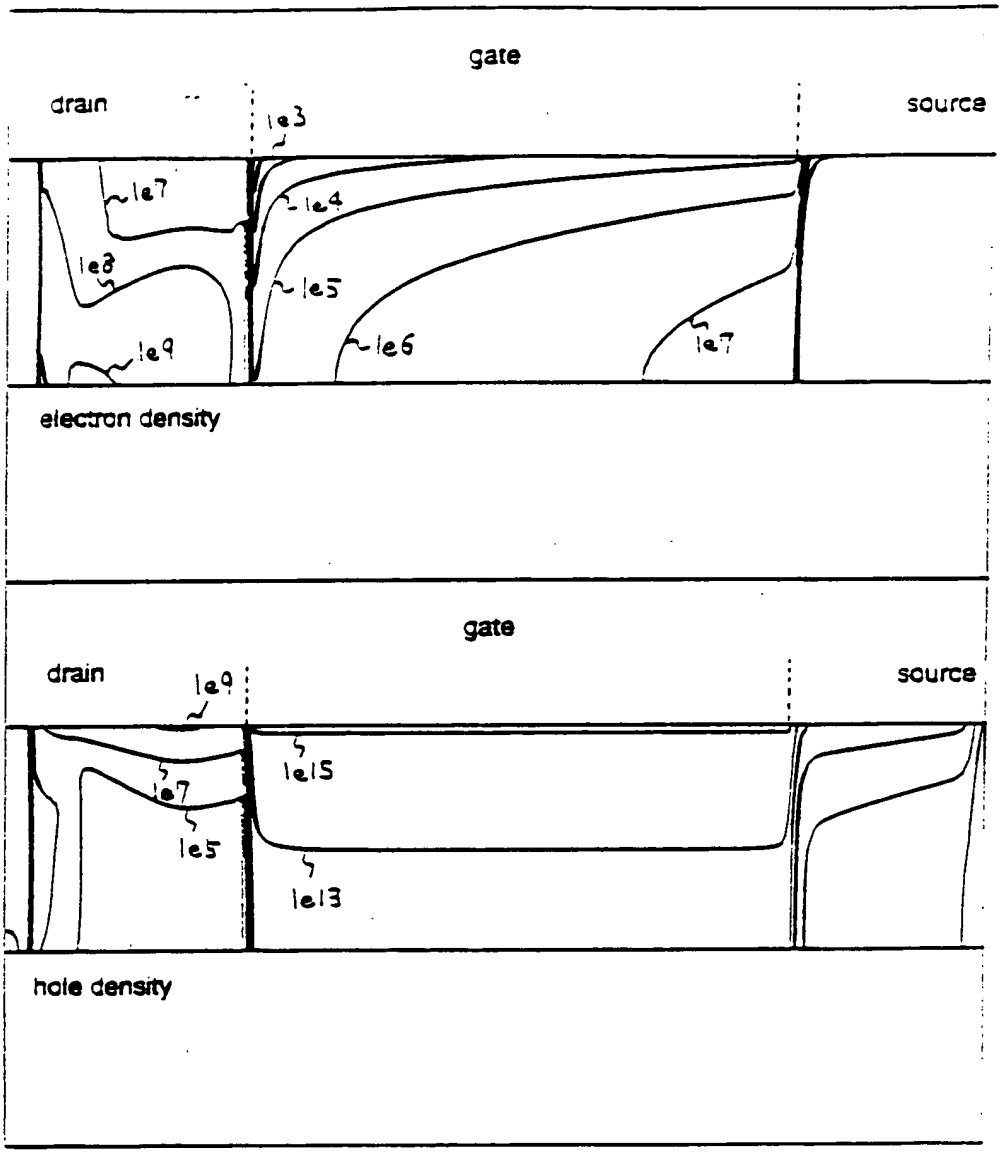

Drain Current (A) : I_{DS}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
10^{-12}
V_{ds}=16V
-10
-5
0
5
10
15
Gate Voltage (V) : V_{GS}
b: LDD 0.5 μm + GOLD 2.0 μm
c: LDD 1.0 μm+ GOLD 1.5 μm
d: LDD 1.5 μm+ GOLD 1.0 μm
a: LDD 0 μm + GOLD 2.5 μm

Fig. 22



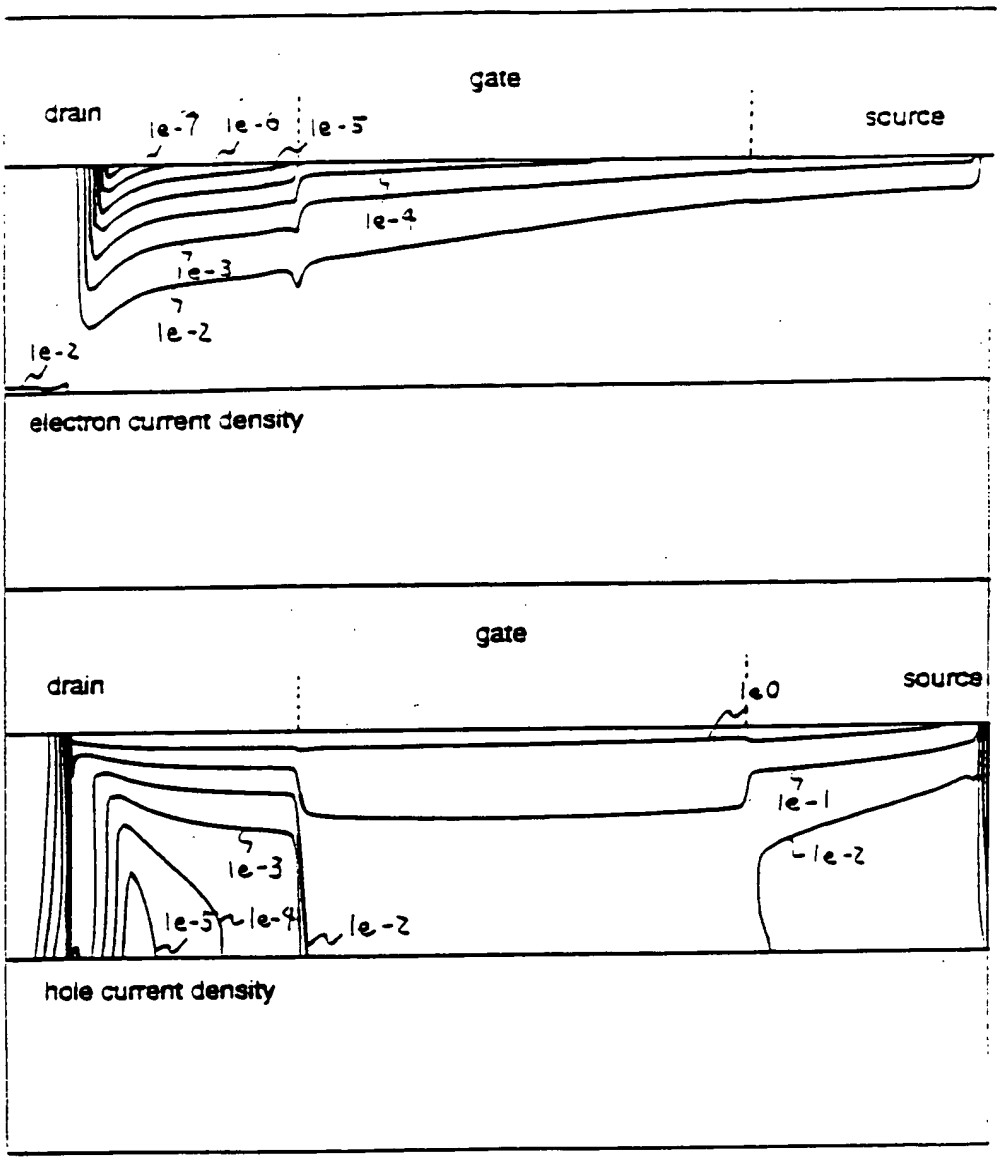
GOLD (2.5 μm) -LDD (0 μm)

Fig. 23



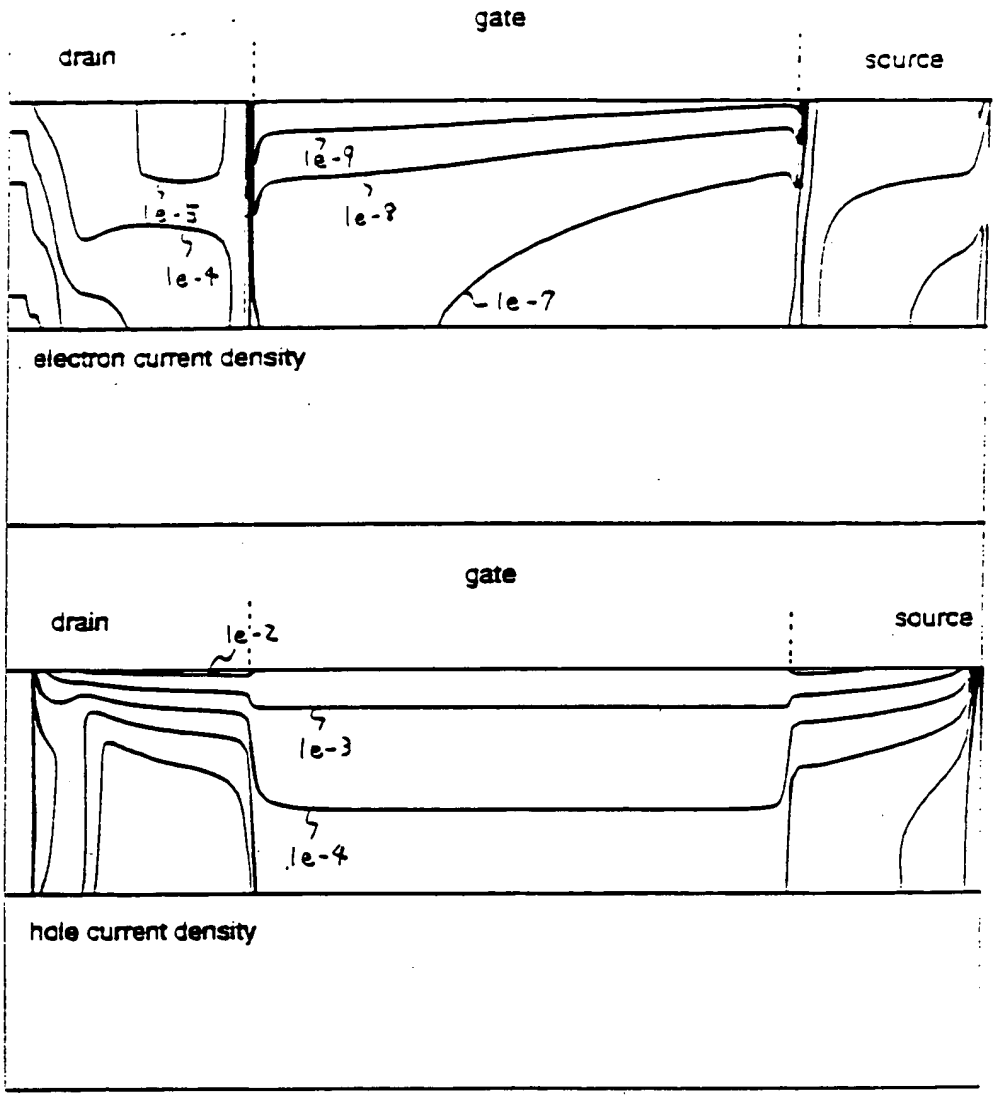
GOLD (2.0 μm) +LDD (0.5 μm)

Fig. 24



GOLD (2.5 μm) – LDD (0 μm)

Fig. 25



GOLD (2.0 μm) – LDD (0.5 μm)

Fig. 26

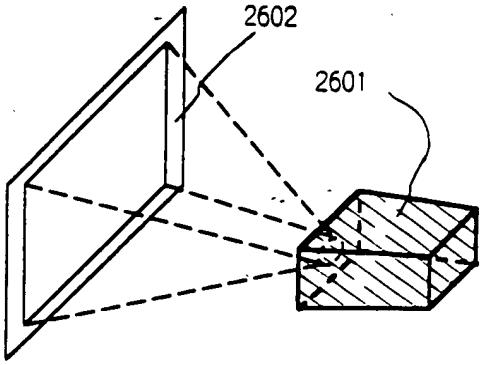


Fig. 27A

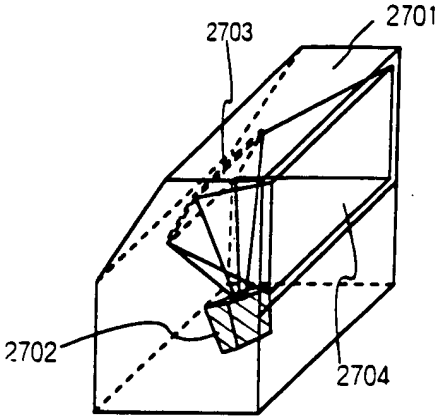


Fig. 27B

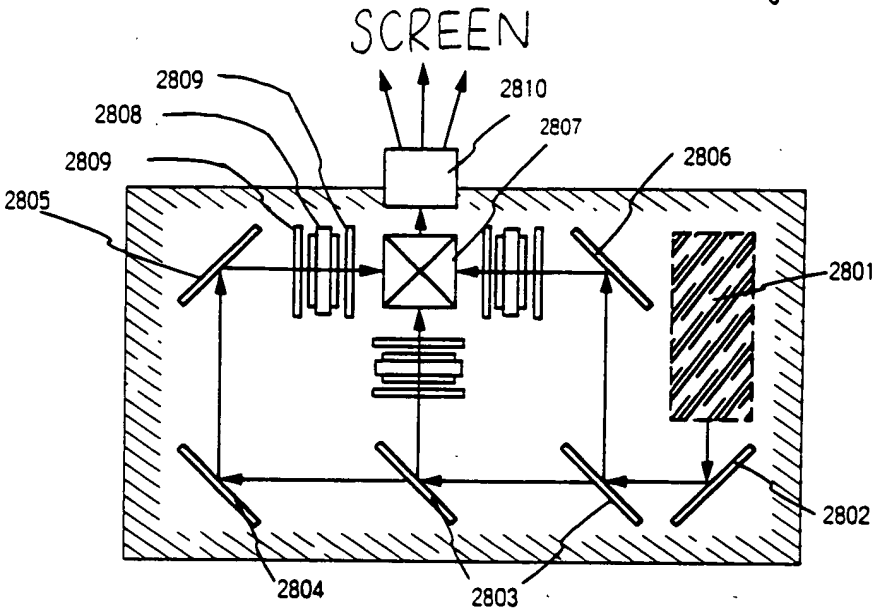


Fig. 27C

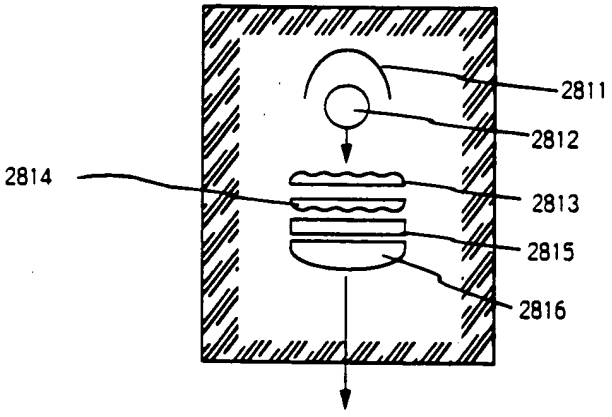


Fig. 27D

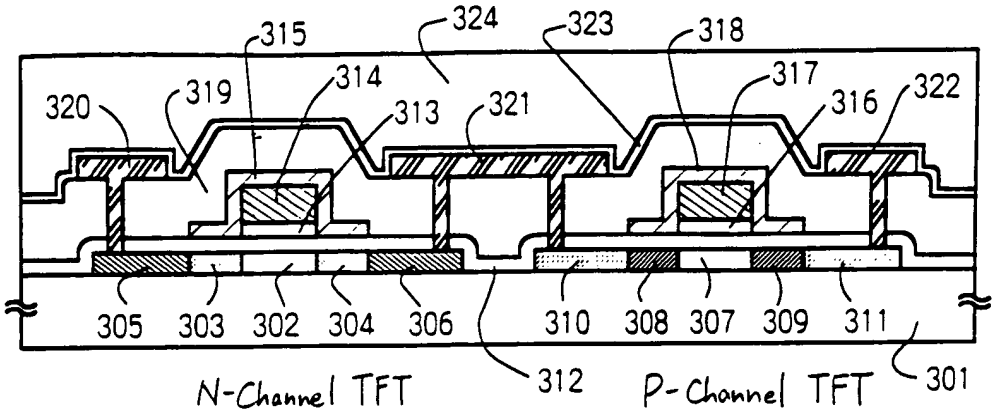

315
324
323
318
320
319
314
313
321
317
316
322
305
303
302
304
306
310
308
307
309
311
312
301
N-Channel TFT
P-Channel TFT

Fig. 28

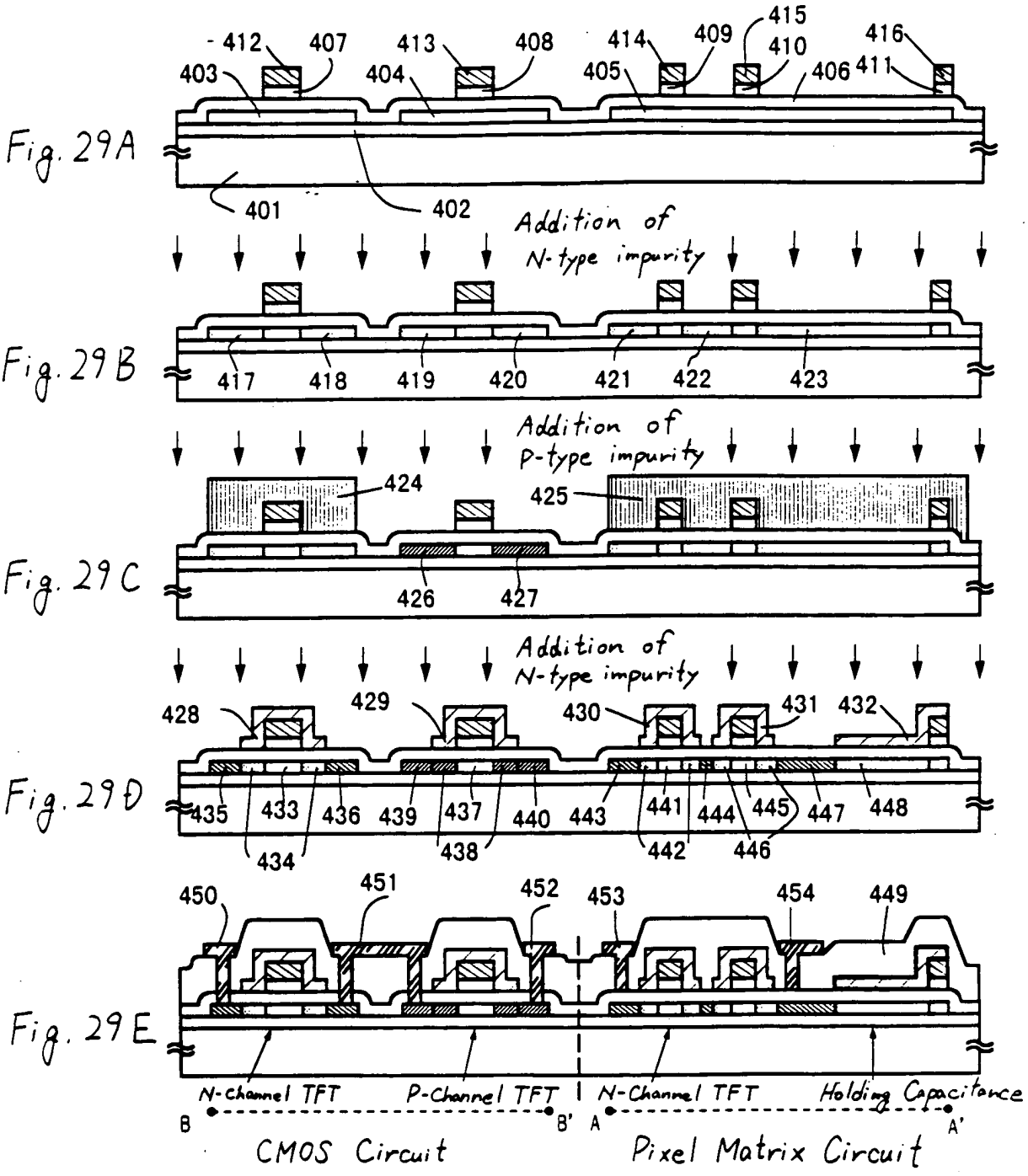


Fig. 29A
412
407
413
408
414
409
415
410
416
403
404
405
406
411
401
402
Addition of N-type impurity
Fig. 29B
417
418
419
420
421
422
423
Addition of P-type impurity
Fig. 29C
424
425
426
427
Addition of N-type impurity
Fig. 29D
428
429
430
431
432
435
433
436
439
437
440
443
441
444
445
447
448
434
438
442
446
Fig. 29E
450
451
452
453
454
449
N-channel TFT
P-Channel TFT
N-Channel TFT
Holding Capacitance
B
B'
A
A'
CMOS Circuit
Pixel Matrix Circuit

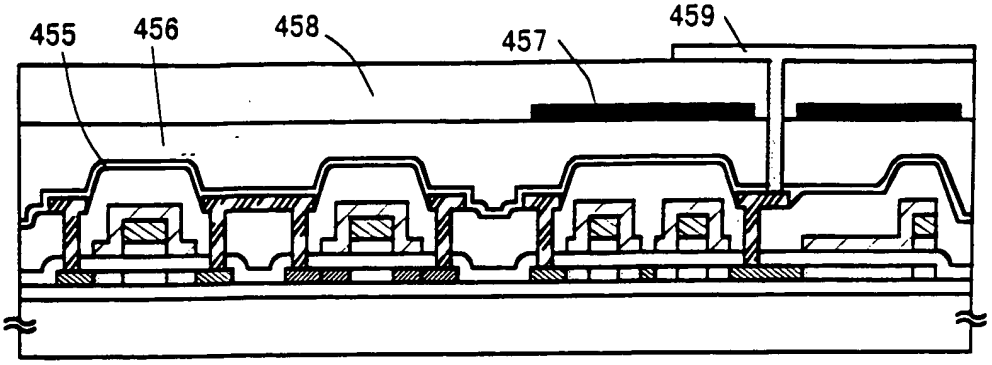


Fig. 30A

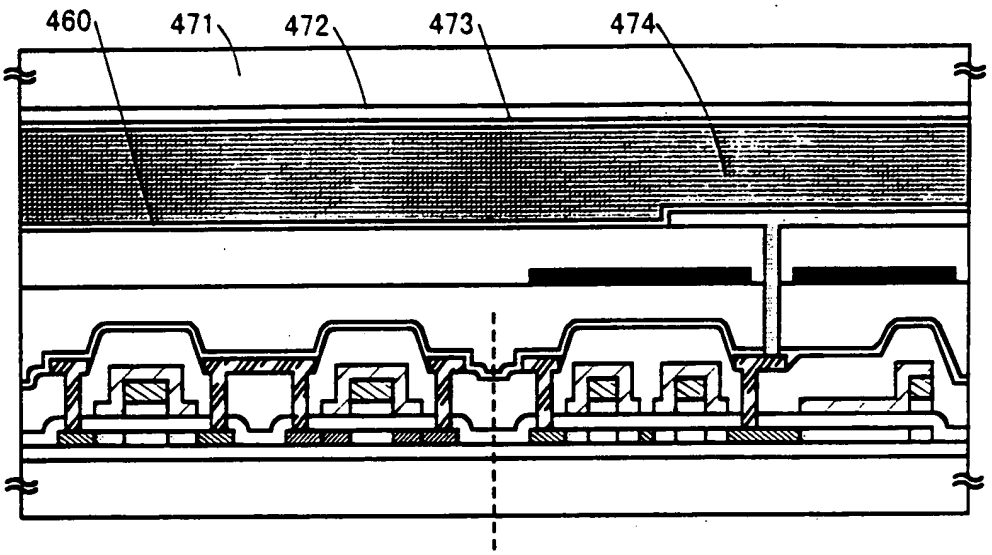


Fig. 30B

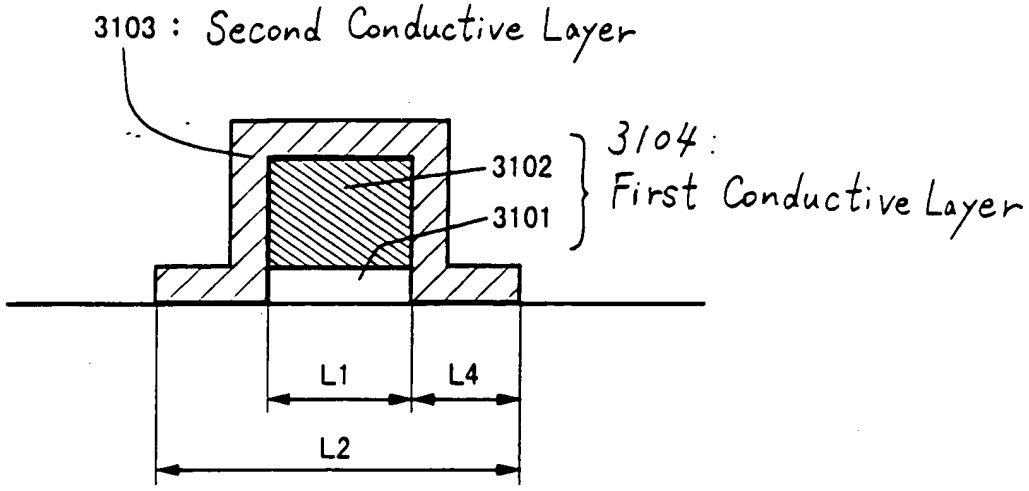

3103 : Second Conductive Layer
3102
3101
3104 :
First Conductive Layer
L1
L4
L2

Fig. 31

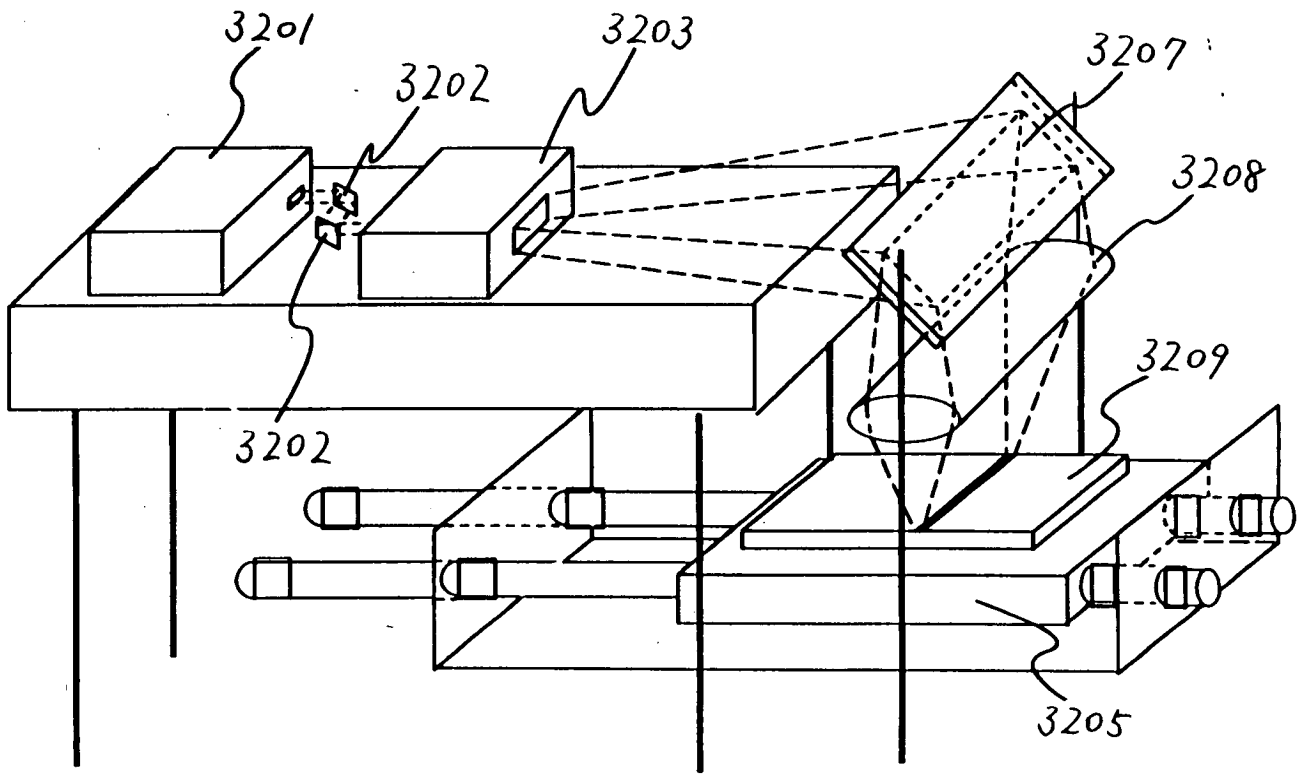


Fig. 32

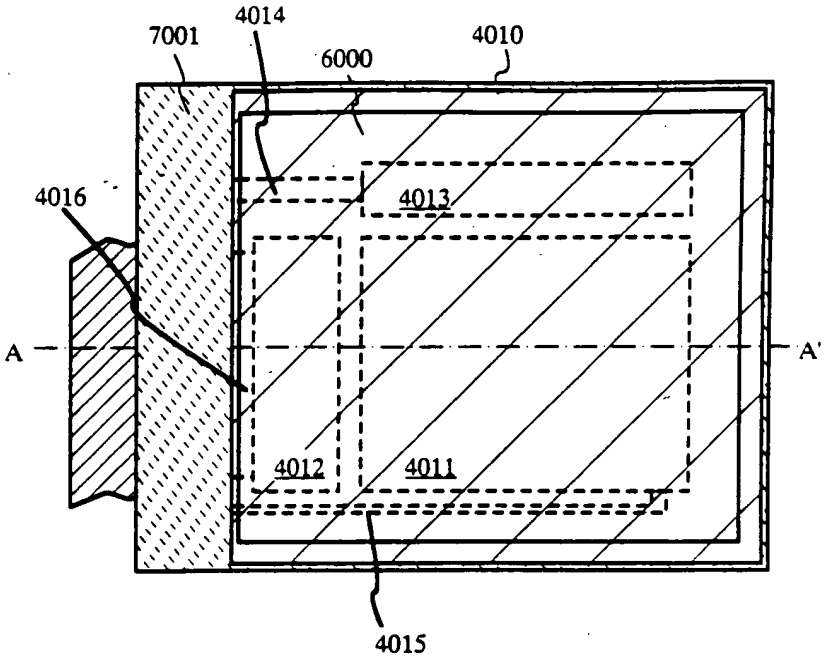


Fig. 33A

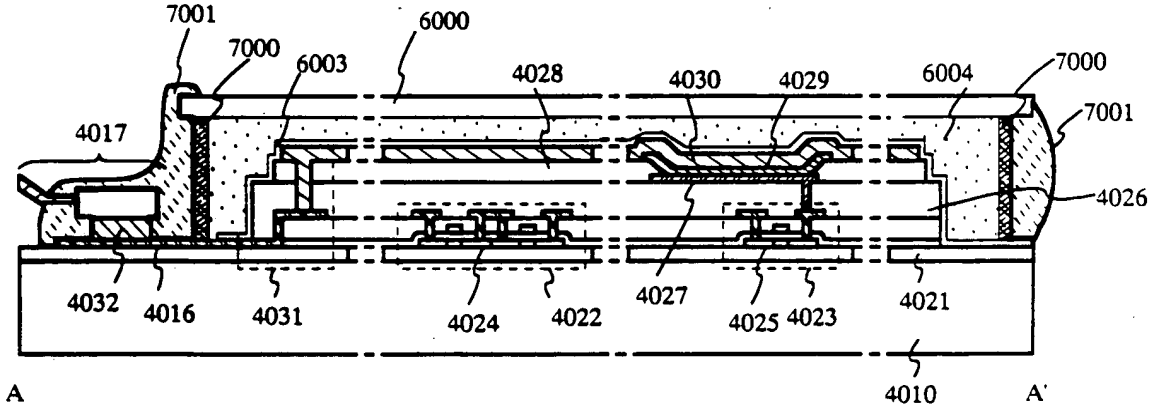


Fig. 33B

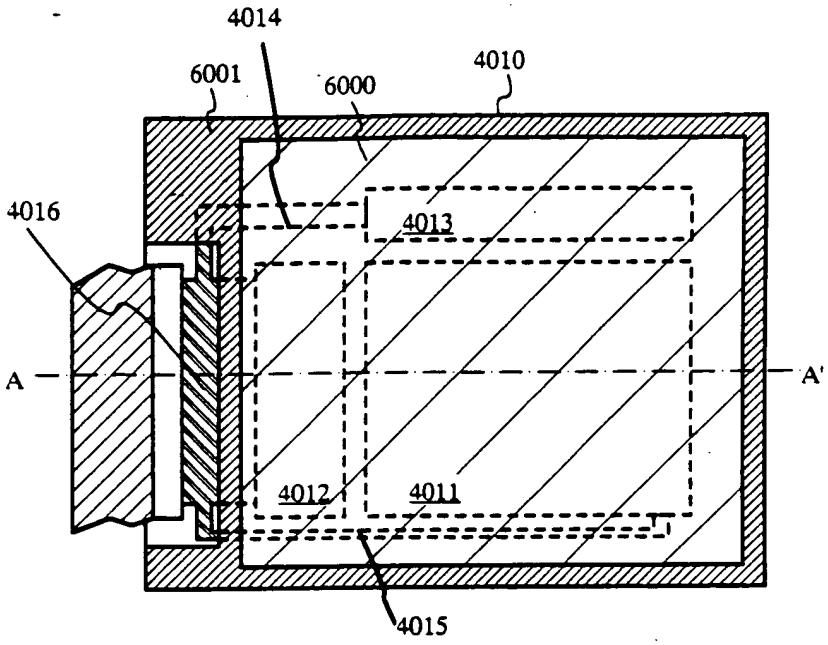


Fig. 34A

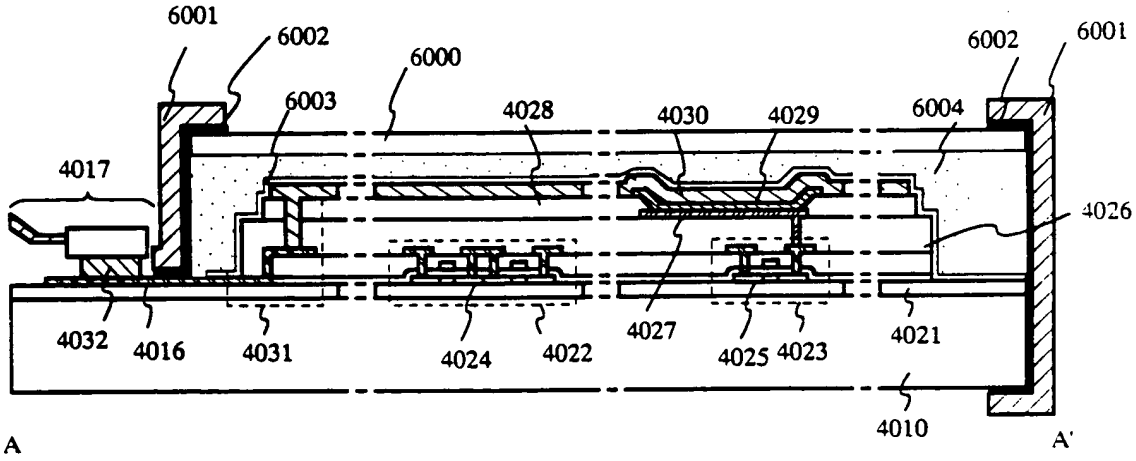


Fig. 34B

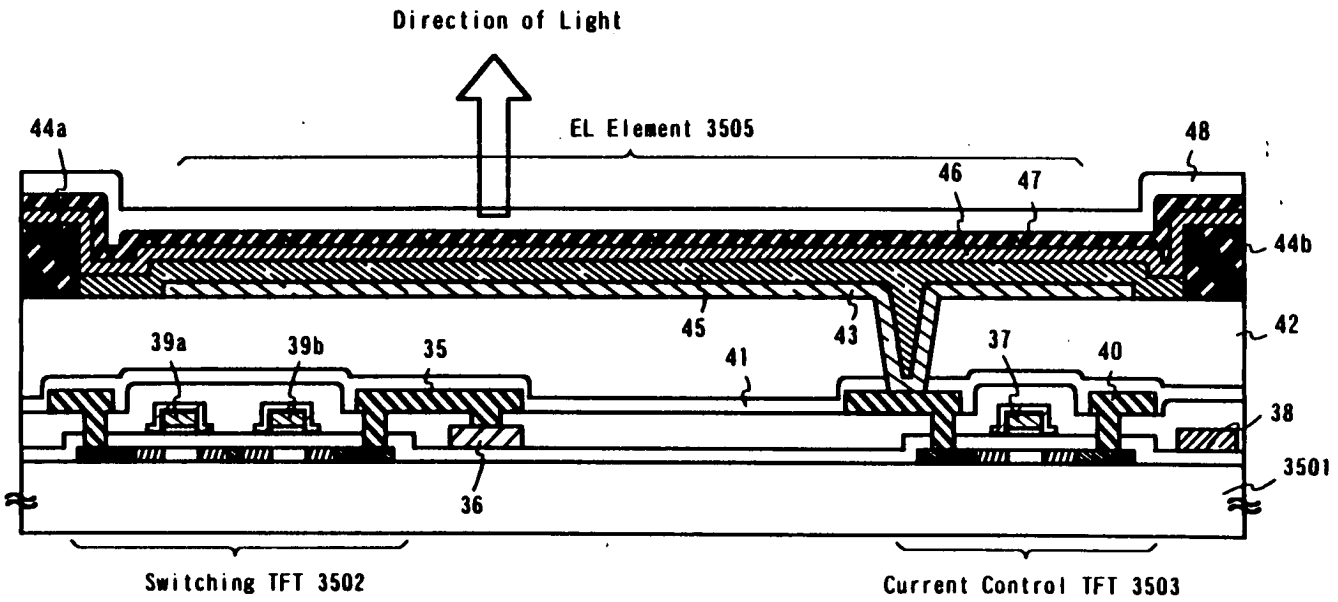

Direction of Light
EL Element 3505
44a
48
46
47
44b
45
43
42
39a
39b
35
41
37
40
38
3501
36
Switching TFT 3502
Current Control TFT 3503

Fig. 35

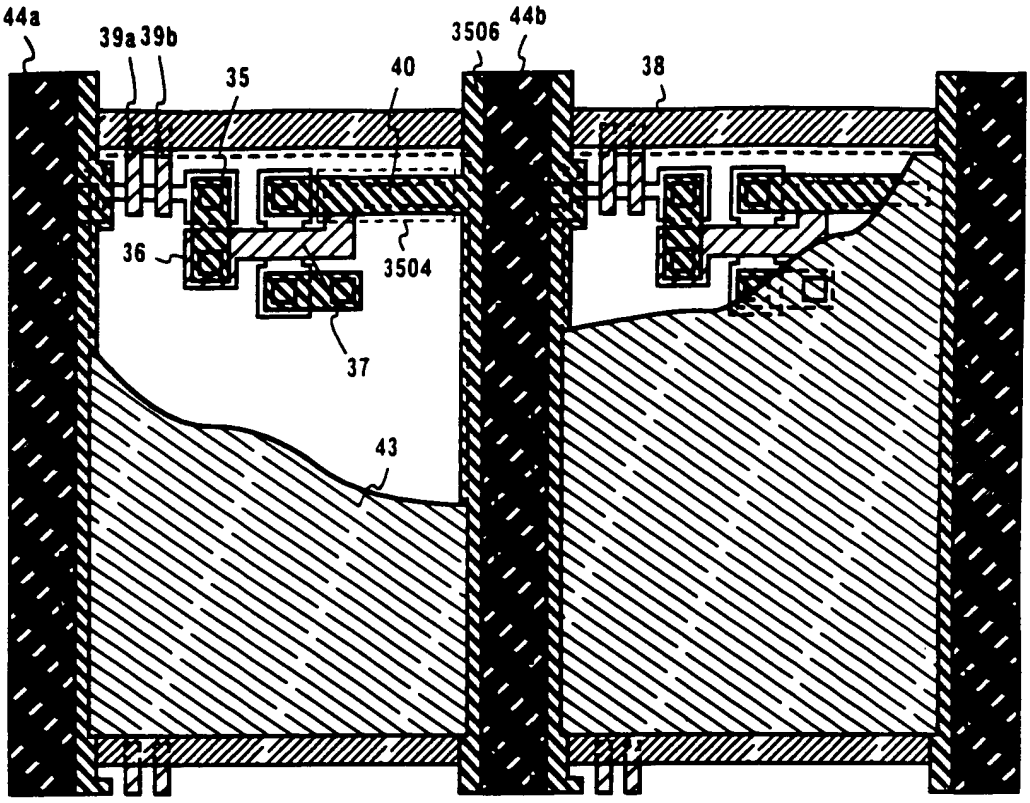


Fig. 36A

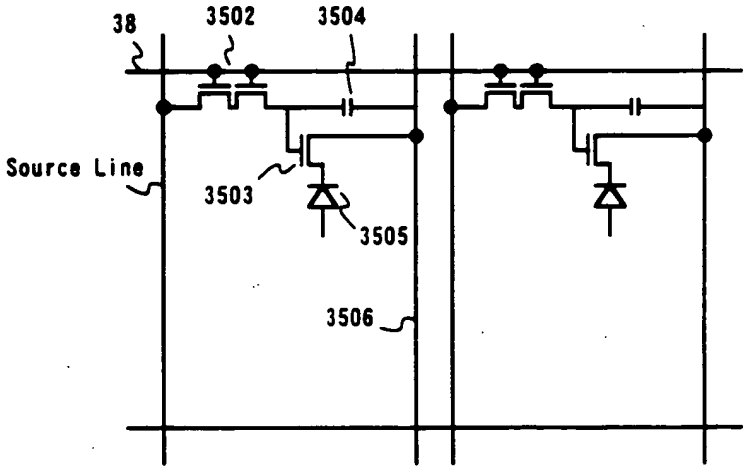


Fig. 36B

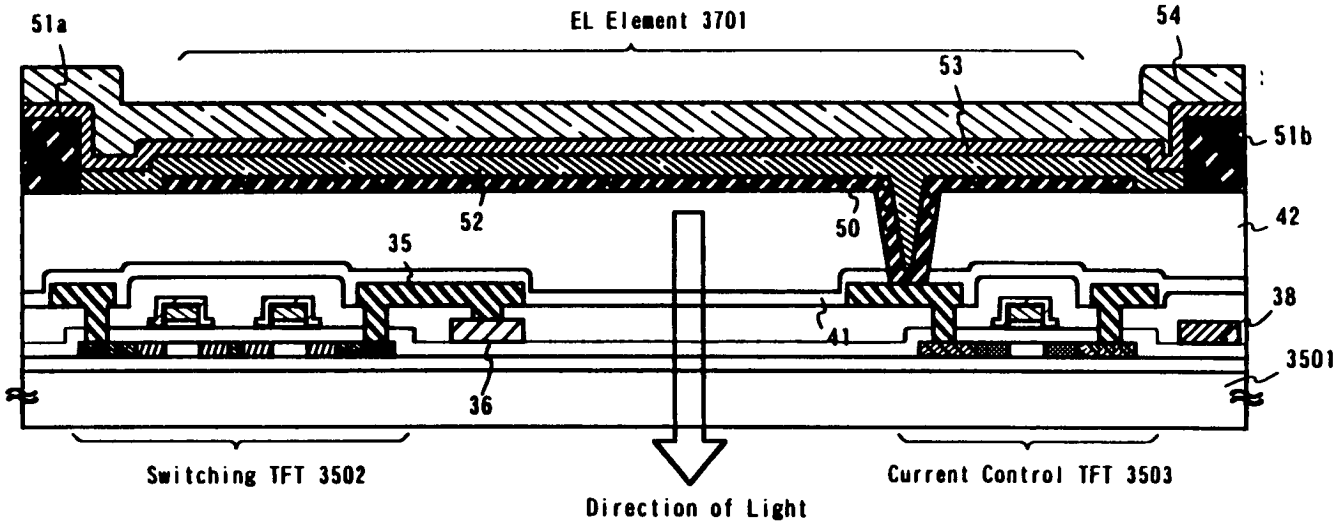

51a
EL Element 3701
54
53
51b
52
50
42
35
38
41
3501
36
Switching TFT 3502
Current Control TFT 3503
Direction of Light

Fig. 37

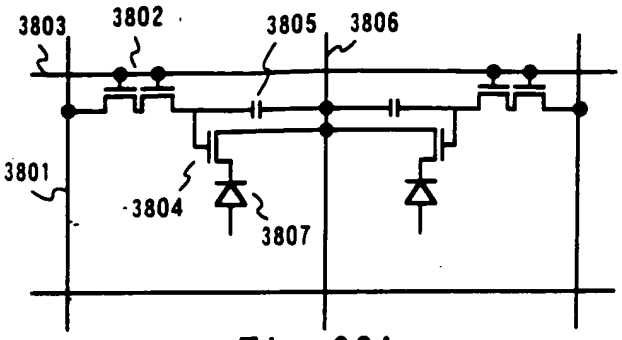


Fig. 38A

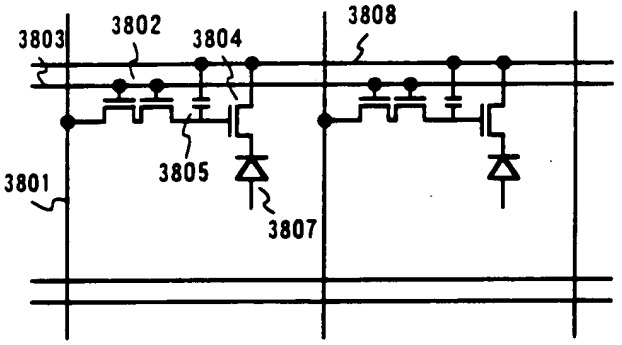


Fig. 38B

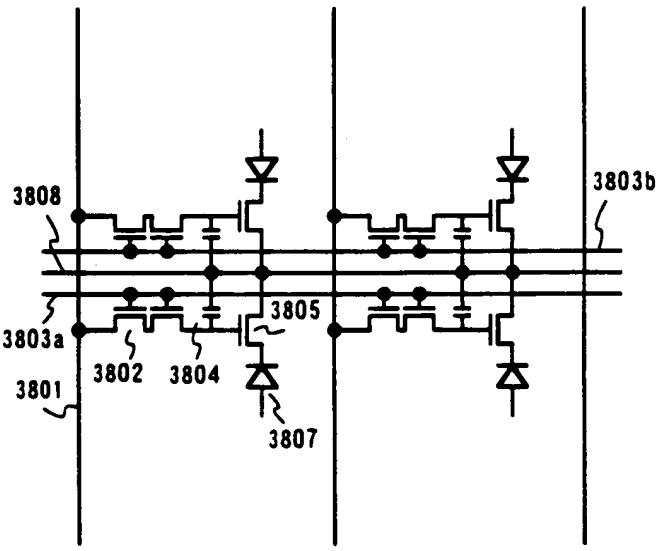


Fig. 38C

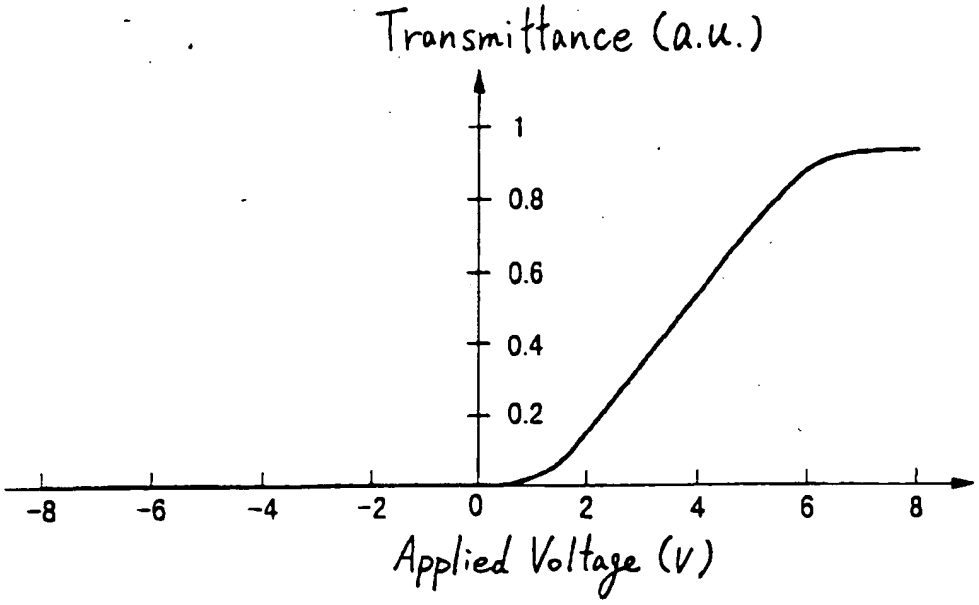


Fig. 39